Muon front-end architecture review report

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Presentations:
http://agenda.cern.ch/fullAgenda.php?ida=a03650

The reviewers would like to congratulate the muon group for having prepared an excellent set of presentations for the review. The general architecture was very well and clearly presented. The general architecture has been found well optimized to read out the large number of physical channels with a minimum number of electronics channels to minimize cost. A large set of test and monitoring functions have been foreseen. The readout architecture seems well planned and the reviewers cannot propose any specific improvements to the chosen architecture.

The readout electronics for the inner part of M1was not presented, as the detector technology is not yet determined (e.g. GEM). It must be assumed that the same front-end electronics, after discrimination of analog detector signals, will be used.

General comments to the chosen architecture

The chosen muon trigger architecture with a 5 out of 5 coincidence imposes strict requirements to the detector efficiency. The use of a wire chamber detector, with drift time and other time uncertainties, require a well controlled timing alignment to ensure that all hits from a bunch crossing are correctly captured within the 25ns bunch crossing interval. High channel efficiency is ensured by first a hardwired "analog OR" between two detector layers (not in M1), before the analog front-end chip, followed by a logic OR between two double layers in each detector station (giving a total of 4 detection layers in station M2 – M5 and two detection layers in M1). An additional level of logic OR-ing is used to generate the logical channels with the granularity needed by the muon trigger. The combination of analog and digital OR's reduces significantly the number of electronics channels for further signal processing but also imposes specific requirements to the front-end electronics. The effective detector capacitance is increased by the hardwired analog OR and the logical OR requires special timing alignment features. Difficult requirements to the dead time (~50ns) of the analog front-end is in addition needed to get good efficiency on channels with hit rates up to 1 MHz.

The general front-end architecture has been made with a strong emphasis on features to allow a good timing alignment of the detector. This specific problem for the muon detector has already been dealt with in a previous review (http://agenda.cern.ch/fullAgenda.php?ida=a01530). The timing alignment of the muon detector is in particular difficult because of the large fraction of out-of-time background hits in certain parts of the detector. The OR-ing of physical channels to generate logical readout and trigger channels also imposes specific features to perform individual time alignment of the physical channels before correctly OR-ing (using simple masking of channels when performing timing alignments). The reviewers appreciate

that the difficult task of the channel time alignment and monitoring is treated with particular care. The reviewers appreciate that the muon group have implemented features to allow an effective time alignment and monitoring. It can be discussed whether the time alignment should be performed on raw hits or off line on triggered events only. The implemented feature of direct time histogramming in the SYNC, on non triggered hits, can though turn out to be a powerful tool for time alignment and monitoring.

The cooling of the front-end electronics inside the detector was not presented in detail. It is planned to use forced air cooling directly to the cavern environment. It should be demonstrated that this is sufficient to remove the dissipated power, guaranteeing an acceptable working environment for electronics and detector. With an estimated power dissipation of ~10 kW in the front-end electronics inside the detector it does not seem obvious that a proper working temperature can be ensured with forced air cooling. It must also be assured that it is acceptable to release this amount of heat into the LHCb cavern. It may possibly be necessary to use a water cooling system, with all the known complications this implies.

Racks containing the digital front-end electronics will be located on the side of the muon detector. Special designed racks will most likely be required to fit six 6U crates and related cooling (heat exchangers and fans) into a single rack. The location of the readout racks for muon station M1 is not yet defined, which may have significant effects on the radiation requirements to the electronics (from ~8 Krad to ~2 Krad) Until a final decision is made it must be assumed that the electronics must be qualified for the worst case radiation environment.

Requirements to radiation qualification of the electronics seem to be well defined. Great care has been taken to select components according to the expected radiation levels. Radiation hard 0.25um CMOS ASIC's are used inside the detector (up to 1 Mrad). For the IB and ODE boards (8 Krad) the components that must be radiation qualified in the near future seems clearly defined. The use of the SYNC ASIC, the GOL link transmitter and ACTEL antifuse FPGA's should assure sufficient radiation resistance. A few components could though become problematic (e.g. parallel optical transmitter containing a EPROM).

For the power supplies a preliminary design study using bulk power supplies a la PL500 (~100A) with power splitting into 10A groups and use of local linear regulators was presented. This will require a more detailed study together with practical tests with realistic loads and cable lengths. Only power at 2.5 volt is needed for the front-end cards. It is assumed that a common digital (for DIALOG) and analog (for CARIOCA) power supply will be acceptable as the digital activity in the DIALOG is minimal (e.g. not clocked during normal running). The proposed power supply scheme with a bulk power source will require a careful evaluation of potential ground loops. Also questions of fusing and fuse reliability must be evaluated if such a big current is drawn from a single power supply channel. The muon group assumes that the bulk power supply is sufficiently radiation tolerant so it can be located in the cavern. The IB and ODE crates will also need radiation tolerant power supplies. The muon group must follow closely (preferable participate in) the radiation qualification and testing of the PL500 or alike (contact: Chris Parkman). Alternative powering schemes must be considered in case power supply units cannot be made sufficiently radiation tolerant.

Grounding of a detector with large capacitances, and therefore working with very small voltage levels, will be critical. At the level of detector chambers and the analog front-end electronics this has been studied in detail, as it has been found to be extremely critical for the stability of the analog front-end. The ground connection of the front-end cards connects to an aluminum bar of the chamber frame as a ground reference. It must be ensured that a reliable contact to the aluminum frame is obtained. A local shield around the front-end electronics is used to exclude external noise sources. Detailed studies will be needed of the grounding at the system level. All test results up to now have been obtained with small and full sized chamber prototypes, where potential grounding problems at the system level may not have surfaced. The fact that differential LVDS signals are-used for signal transmission over distances up to 10 m, should contribute to reduce global grounding problems.

The analog front-end chip CARIOCA, just recently reviewed (http://agenda.cern.ch/fullAgenda.php?ida=a03311), is a critical component for the muon detector. This chip uses the 0.25um CMOS technology, which has been used successfully for several other LHC

preamplifier-discriminator systems. It is known to be rad-hard, cost-efficient and giving high and stable production yields. Electrical stability problems of the analog front-end have been encountered in previous versions of the CARIOCA chip for certain operating conditions. The reasons of these problems seem to be understood, and it is expected that a newly submitted version will resolve these problems. A backup solution using the ASDQ chip, with a separate external transistor input stage, has been used extensively for chamber characterization. The bipolar technology used for the ASDQ chip is though very expensive (an additional cost of ~700k CHF is estimated). Front-end cards for both CARIOCA and ASDQ are developed in parallel, until a final front-end chip decision is made by the end of 2003. The reviewers encourage the CARIOCA team to develop the chip up to a successful end. There seems to be no technical reason, why the CARIOCA chip should not work up to design specs, as 0.25um CMOS is a mature technology and has been demonstrated to give excellent results in other LHC related experiments. The main problem seems to be availability of sufficient manpower with the required analog design expertise. The ASDQ has been used for characterizations of the different chamber configurations. Before the CARIOCA can be considered sufficiently mature it must be tested extensively with all the different chamber configurations.

Prototypes of the DIALOG ASIC have been tested and have for main functions been found to work as required. A Final version will need 16 DAC's plus a low impedance output driver for supplying thresholds to CARIOCA or ASDQ front-end chips. The DIALOG has full triple redundancy for SEU correction. The use of an I^2C chain of up to 10 DIALOG chips gives a certain risk of loosing a whole chain of chips if a bad connection occur (not considered critical).

Service boards, handling the interface from front-end modules to the ECS system, have been prototyped and are currently under test. No specific problems have been encountered with its function. ELMB software and the PVSS interface remains to be finalized. If the service board is used in racks on the sides of M1, the radiation tolerance of the ELMB is marginal (can possibly be exchanged after a few years if spares are available).

IB boards based on antifuse FPGA's have been prototyped and tested. Ensuring a god delay matching is critical as delay skews at this level cannot be fully corrected for by the programmable delays in the DIALOG. Only minor optimizations in the FPGA programming are needed.

The SYNC TDC ASIC has just been prototyped and will be tested in the coming months. It is based on the same basic timing circuit that has already been verified in the DIALOG. Verification tests of a FPGA version are currently ongoing. The SYNC has full SEU protection using triple redundant registers and hamming-code protected memories. As this is the first prototype version of the ASIC any problems encountered in its testing could become critical for the planned time schedule.

The ODE board layout has been made and will be tested with SYNC FPGA's and finally with the SYNC ASIC when available. Different detector configurations are handled by a motherboard using 3 different types of plug-in cards. The board controller is currently based on a Xilinx FPGA to allow quick reconfigurations to be made. In the final version an antifuse FPGA will be used for SEU immunity reasons. Extensive SEU protection schemes are envisaged and multiple test and monitoring features are planned. Many of the planned features are nice to have but will make the FPGA implementation more complicated. All planned features must be fully verified to work correctly, otherwise simplifications should be made. It is planned to use the new AX series of antifuse based FPGA's. It is recommended that the muon, calorimeter and RICH groups get together to discuss the use of this FPGA family in radiation environments.

The requirements to the L1 front-end electronics seem compatible with the use of the common L1 front-end module. The use of this module will also allow muon information to be used in the L1 trigger as the common L1 front-end module has processing capabilities and links available for this. The required processing on the L1 module seems well covered by the FPGA resources available. It is proposed that the muon group contributes to the common L1 specification document with a chapter on details about its use in the muon detector (input data format, zero-suppression, number of modules needed, etc.).

Planning

A critical part of the general planning is the design, test, and qualification of the three ASIC's needed in the muon detector. The planned submission of all three ASIC's on the same production run introduces a strong dependency between the three ASIC's. A delay in the design of any of the ASIC's will delay the others. The CARIOCA being a tricky analog design could easily become the critical component. The SYNC ASIC could also be critical, as the first prototype version will be tested for the first time in the near future. The current planning of having all three ASIC's ready for production in the end of 2003 seems too optimistic.

Coming reviews

With the presented planning for the production of the front-end electronics all ASIC's and board designs have to be ready for production end 2003 – begin 2004. As all ASIC's must be produced together it can be proposed to have one common production readiness review for all three chips. A common PRR for the different boards also seems reasonable.

CARIOCA, DIALOG and SYNC PRR:	December 2003
FE card, IB, ODE, SB PRR:	February 2004