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TGC Chambers for the LHCb Muon Detector

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Abstract

The technology of Thin Gap Chambers offers a flexible, safe and well tested solution for the LHCb muon detector. These chambers have already been extensively studied and tested (Ref. Atlas muon TDR) operating with a highly quenching and relatively high gain gas mixture. We have tested on beam 2 prototypes of double gap chambers adapted to the LHCb requirements. One of the prototypes was operated with a front-end board using the ASD (Sony) chip adopted by Atlas. The efficiency, time and space resolution and rate capability measured with this prototype are well matched with the LHCb requirements, even in the higher rate and higher resolution regions. This prototype with minor modifications is a good candidate for most of the muon detector. However for ageing reasons, where the particle flux is very large (certainly in M1), a solution with chambers operating at a lower gas gain and a different solution for the front-end should be found. The project for those regions need further study. Tests are under way.

Here we propose a detector design for stations M2-M5.

1 Introduction

Thin Gap Chambers have a structure similar to multi-wire proportional chambers except that the wire to wire distance is larger than the cathode to anode distance. The cathode is resistive and is obtained with a graphite varnish on a G10 layer (see fig.1) The signal can be readout directly on wires. The signal induced through the resistive layer on conductive electrodes lying on the other side of the G10 layer can also be readout.

The "TGC technology" permits to build in a simple, cheap and safe way, wire chambers with STRIP or PAD readout. The production procedure is well adapted to build small chambers (without wire spacers) as well as chambers having the maximum dimensions foreseen in the muon detector matching with the requirements given by occupancy and time resolution (up to 1.2×1.5 m^2). This allows to minimize the total number of chambers to be built and operated, and also the zones of chambers overlap. Double-gap chambers with staggered wires can be easily realized. In double-gap chambers physical channels, wires and strips, can be directly ORed on the chamber or alternatively the signal from wires and strips can be sent to the front-end board sitting on the chamber edge and the output ORed. The first solution is convenient from the point of view of cost, but the second one could be convenient for safety reasons and trigger efficiency.

TGC have been operated with a gas mixture based on CO_2-n-pentane. The n-pentane has been used as a quencher in order to operate the chamber in saturated avalanche regime without any streamer pulses. This regime provides a good timing resolution and a good rate capability. The chambers have been continously flushed with 55% CO_2 and 45% n-pentane, the standard ATLAS gas mixture, at an overpressure of few mbar.

- TGC provide a time and space resolution matching the LHCb requirements. In particular the small distance between anode wires and cathode (1.4 mm) provides a good intrinsic spatial resolution permitting the use of small size logic channels as the ones needed in the inner region of the detector.

- the distance between wire planes in a double gap can be as small as 0.6 mm and even less for strip to strip. This allows better performance in time resolution when using staggered wires and in signal to noise rejection using an OR and eventually AND logic.

- the graphite cathode makes a uniform screen to the conductive electrodes, thus reducing the problems coming from mechanical deformations and the necessity of building very precise/smooth cathode electrodes with relatively expensive techniques. Moreover, the cathode electrodes are "external" (not in contact with the gas) and this allows an easier (cheap and safe) access to the electrodes from the front-end which is particularly usefull in case of pad read-out. This feature facilitates the construction of large size chambers composed of small size logical entities, as required by occupancy and trigger performance

- the use of a quenching gas mixture, together with the TGC cell geometry allows operation in saturated mode. This mode has the advantage of making the chamber less sensitive to geometrical/mechanical tolerances which is relevant for large detectors (ref. p.316 of ATLAS Muon TDR). The mip signal has a small dependence on the incident angle up to angles smaller than 40 degrees. This is relevant in the LHCb environnement because most of the background hits, although being generated by large angle tracks, will give signals similar to the ones of perpendicularly crossing particles. Landau tails are small, in particular the response to slow neutrons is similar to that of mip's (ref. ATLAS). No streamers are observed in any operating condition. This ensures stable running conditions with limited charge deposit per particle.

- TGC can be operated with the Sony ASD chip, providing a satisfactory time resolution. Our tests have proved that TGC perform well at the higher rate foreseen in the muon detector. Nevertheless ageing reasons impose a "low gain solution" for the high rate regions and a solution is under study. Operation at low gain requires also further studies for the front-end electronics.

2 Layout

The size of logical pads and strips has been decided conditioned by the wanted spatial resolution and by the occupancy. In the regions having large logical channels, they are composed by the OR of several physical channels whose dimensions are decided taking into account capacitance and rate. The maximum strip length is also conditioned by the wanted time resolution.

We do not present any solution for M1 station. We propose to equip all the stations M2–M5 with one double-gap chamber, each gap having a system of wires and orthogonal strips. For redundancy, the stations M2 and M3 are be equipped with two double-gap chambers.

In fig.2 is reported the chambers layout for one quadrant and the total number of chambers. Only 3 different chamber sizes per station are considered.

In fig.3 we report the layout of physical channels, valid for all the stations and the total number of physical channels.

In fig.4and in fig.5 we report the logical channels layout for M2 M3 and M4 M5 respectively.

In the stations equipped with 1 double gap chamber the logical channel is the OR of the two corresponding channels of the two gaps. In the stations equipped with 2 double gap chambers, the logical channel can be any majority of the channels of the four gaps. Simulation with the new background parametrization must be performed to study the convenience of a majority logic. The result of the study can bring to different solutions for the best chamber assembling in the station mechanical structure. Preliminary results indicate that the best performance is obtained with the minimum distance between the corresponding elements to be OR'ed, AND'ed.

3 Performance required

- Time resolution

  The time resolution must be such to permit bunch crossing (BC) identification (<25 ns) for ∼99% of the hits for each logical channel (OR or majority of physical channel). For each physical channel, chamber time jitter + front-end electronic time walk + signal propagation on wires and strips + electronic jitter in the signal transmission and syncronization contribute to the final time resolution. In wire chambers the time jitter distribution is not gaussian, with very long tails, so a full simulation of the various contributions had to be performed in the Monte Carlo to study the effects on the trigger performance. Preliminary results of the simulation indicate that the wanted efficiency in the BC identification is reached if strips are less than 1.5 m. in length and that more than 99% of the events in the experimentally measured time jitter distributions for logical channels lie in a 20 ns time window.

  As an example in fig.6 is shown the overall time-spread distribution for all the logical channels fired by muons (in B $\rightarrow \mu +$ X events) with a $p_t > 1.1$ GeV/c. In this simulation the maximum length of the strips was 1.5 m (while in the proposed layout it is only 0.75 m), only one layer (two gaps ORed) in all the stations has been assumed and the distance of the two gaps is 10 mm. The application of a time-gate of 20–25 ns results in a relative loss of trigger efficiency for this type of events of 6–0.8%.

- Chamber efficiency

  The efficiency per each chamber gap must be such to give an efficiency per logical pad > 99%. Due to the fact that, for time resolution reasons, we require the OR of two gaps, the efficiency requirement for each gap is not very stringent: a single gap efficiency better than 95% is sufficient.

- spatial resolution / cross talk

  The experiment requires a logical read-out of wires and strips which width varies from .6 to several cms depending on regions.

  The hit cluster size must be near to 1 to avoid spoiling the detector performance in the areas where physical channels coincide with logical channels. In the areas where a logical channel is formed by the OR of several physical channels, the condition is less stringent.

- rate capability

  see Burkhard table upgraded with the new background

- radiation tolerance/ageing

  see Burkhard table upgraded with the new background

4 Prototypes characteristics

Two different prototypes have been built and tested on beam. The two prototypes are derived from the ATLAS TGC trigger chambers with modifications in the cathode design and in the graphite layer resistivity to match the LHCb requirements. The two prototypes have been assembled at the Rehovot Weizmann Institute in Israel.

In fig.1 is shown a schematic picture of a TGC. Both prototypes have a double gap with staggered wires and a resistivity of the graphite layer of 200 kΩ/sq matching the high rate capability required. The graphite layer is connected to ground through two small copper contacts (a better contact all along the chamber frame, further improving the rate performance, is foreseen in the final chambers). The gap width (distance wires-graphite layer) is 1.4 mm. The wire diameter is 50 μm and the wire pitch is 1.8 mm. In both prototypes the wires are grouped in groups of ten. In the following such group of wires will be called "wire". One channel of high voltage provides the voltage of a single gap. The voltage is distributed to each wire through a 10 MΩ resistor, the output signal from the wire is decoupled to the high voltage by a 470 pF capacitor. The chamber dimensions are in both cases 80$\times$30 cm^2.

The two prototypes (A and B) have different construction characteristics. Prototype A is the standard high resolution ATLAS muon trigger chamber. It has 0.2 mm of G10 between the graphite and the conductive electrodes and 1.6 mm of G10 between electrodes and the ground plane (fig.7). The wires are 30 cm long and the strips 80 cm. The strip width is 3 mm and the inter-strip gap is 0.2 mm. No wire spacers are used.

Prototype B has 1.6 mm of G10 between the graphite layer and the cathode electrodes and 5 mm of paper honeycomb between electrodes and ground plane (see fig.8). Wires are 80 cm long and spacers are used to avoid wire displacement. One gap is equipped with 30 cm long strips, the other one with different size pads. The strips width is 13 mm and the inter-strip gap 2 mm, the pad dimension is variable from 1x2 cm^2 on (see fig.8). Prototype B has a slightly poorer electric performance (see later) but offers an easier access to the pad and a lower production cost.

4.1 Front-end electronics

For prototype A we used the "old Cardarelli" test front-end (preamplifier + MAN voltage amplifier). This electronics is not a candidate for the final front-end solution. The ATLAS TGC Amplifier and Shaper Discriminator (ASD made by Sony) [1] was used for prototype B. The ASD chip first stage is a charge amplifier with an integration time of 16 ns and a gain of 800 mV/pC. The amplified signal is then sent to a linear voltage amplifier ($\times 7$), discriminated and shaped according to the LVDS standard. No analog output is provided by the chip which foresees a remote threshold setting.

5 Beam test setup

A preliminary test has been done at the X7 area of the CERN SPS with the prototype A. During this test only one channel of a single gap was instrumented and no cathode electrodes were read-out. Three scintillators counters were used as trigger for the DAQ. A small counter defining an active area of 1 cm^2 was used for the TGC efficiency measurement. The signal coming from the front-end was amplified, discriminated and sent to the DAQ (TDC and ADC).

The prototype B has been tested at the T11 area of the CERN PS. The DAQ trigger was given by the same scintillator counters system. A beam hodoscope made of 16 scintillators 1 cm wide (8 in the horizontal direction and 8 in the vertical direction) was used for efficiency measurements. The number of channels instrumented during this test was:

- 16 channels of wires (8 for each gap)
- 8 channels for strip electrodes
- 8 channels for pad electrodes

6 Results

6.1 Efficiency

At the SPS test beam the TGC efficiency (prototype A) was measured using the small counter. The wire ADC distribution (fig.9) shows a well separated signal peak with respect to the pedestal. The threshold applied to the signal (15 mV) corresponds to 350 ADC channels. The efficiency was measured recording the number of counts of the small counter and the number of counts of the coincidence between counter and wire (group of 10 wires 18 mm wide). A cut on the ADC of the trigger scintillators has been applied to avoid multiple track events. The efficiency curve in function of the high voltage applied to the chamber shows (fig.10) a plateau of about 600 V with an efficiency in the plateau region $> 99\%$.

During the PS test beam the efficiency of the TGC (prototype B) was measured using the informations of the beam hodoscope. The efficiency is measured recording the number of tracks with only one vertical and one horizontal hit on the hodoscope strips and the number of corresponding tracks with one single hit on TGC in the region interested by the beam spot. The same procedure was applied for wires and cathode electrodes. In fig.11 we show the efficiency curves for the wires of the two gaps, for strips and pads as a function of the high voltage applied to the wires. We set a threshold of 300 mV for the wires and of 250 mV for electrodes. Lower values for the thresholds were unreachable due to the instability of the ASD chip. All the curves show a plateau with an efficiency greater than 99%. The high voltage plateau for the wires must be compared with the one obtained at the SPS test beam with the different front-end electronics. The plateau for wire of prototype B (fig.11) is about 100 V longer than that of prototype A (fig.10) and this can be easily explained by the better threshold setting.

For strips and pads the signal amplitude is lower than for wires. The signal on the cathode electrodes is a factor 2 lower and for the strips there is an additional factor 2 caused by terminators that we put on the strips to simulate a correct operation of strips much longer than 30 cm. This explains the shorter plateau for strips and pads because the lowest threshold we could apply was still too high. (It must be noticed that in the presently proposed layout, the maximun strip length is only 0.75 m and in the detector regions subjected to high radiation, where ageing problems suggest to work at low voltage to reduce the gas gain, strips are very short and do not require terminations.)

The efficiency measured shows us that the TGC can operate at a voltage as low as 2.9 kV with an excellent efficiency on the wires with the present front-end electronics. Improvements are foreseen in the ASD board design: better high frequency screening of the ASD chip and better decoupling of the threshold input with respect to the LVDS output to avoid oscillations. These improvements will permit to work at a lower threshold for strips and pads and to reduce the chamber operating voltage.

6.2 Time jitter

The time distributions measured in the two tests beam are shown in fig.12. For both prototypes we achieved a RMS of the time distributions of the order of 6 ns and 99% of the events are in a time window of 25 ns.

For prototype B we have performed a software OR of the time signal of the two gaps and we have done measurements at different inclinations of the tracks with respect to the wire plane (fig.13). For all the inclinations checked, 0°, 4° and 15° degrees, more than 99.5% of events are contained in a 20 ns time window satisfying the time resolution requirements.

In fig.14 we report the effect of applying a gate of 25,20,15 ns on the efficiency curve for wire OR of the bigap.

The measured time jitter is the convolution of the chamber intrinsic time response fluctuations due to the electrons time drift and the electronics time walk. The time walk of the ASD Sony chip has been simulated, assuming different values of the charge per particle and different thresholds (see fig.18 and fig.19). The simulation indicates that the Sony chip is well matched with the experiment time resolution requirements when working with a TGC operating at a relatively high gain. The possibility to use the same front-end with a chamber operating at a much lower gain should be further investigated.

The experimental variations of the time distribution mean value and R.M.S as functions of the high voltage for wires, pads and strips are shown in fig.15. In fig.16 is shown the correlation between the TDC of one wire and the TDC of the corresponding strip. The correlation is linear as expected and the large tail in the region $T_{strip} > T_{wire}$ is essentially due to the too high threshold for strips.

In conclusion, for the proposed layout, the resolution measured on prototype B equipped with the SONY ASD is well matched with the performance required.

6.3 Cross talk and cluster size

We define cluster size the number of adjacent physical channels fired by a single track. The cross talk between adjacent channels is the main contribution to the cluster size.

We have determined the cluster size by looking for tracks with only one hit in one horizontal and one vertical hodoscope strip. For such tracks we counted how many adjacent channels have been hit. We applied this procedure separately for wires, strips and pads and the cluster size as a function of the applied high voltage is shown in fig.17 together with the efficiency curves. The width for wires, strips and pads is 18 mm, 15 mm and 20 mm respectively. For a high voltage of 100 V above the knees of the respective plateaus the wires have a cluster size of 1.05 and the cathode electrodes a cluster size of 1.2.

A P-Spice simulation of the two TGC prototypes having gaps equipped with strips (13 mm width, 2 mm interstrip gap) has been performed. The cluster size is well reproduced. In fig. 20 and fig. 21 are shown the crosstalk and efficiency vs. threshold for prototype B. From these figures we can easily evaluate the cross talk for smaller size strips. The simulation shows that the cross-talk can be reduced using the geometry of prototype A (different ratio between graphite-strip and strip-ground capacitance). See fig. 22.

Anyway even assuming the measured performance of prototype B, the cluster size is adeguate to a good trigger performance. If one scales the measured value to the sizes of the logical channels of the proposed layout, the cluster size in region R1 of M2, M3 becomes about 1.1 both in X and Y and not significantly different from 1 in all the other regions.

6.4 Gas Gain Evaluation

When testing the prototype A two different measurements of the charge deposited per mip have been done. With a nano-amperometer we measured the current I driven by the power supply during the beam spill and the out of spill current I_0. The beam rate R was measured using large scintillator counters and assuming an effective spill duration of 2 s. The charge/mip is defined as $(I - I_0)/R$ and results to be of order of 10 pC per mip at 2.9 kV (fig.26a). The measurement is affected by large systematic errors on the absolute amperometer calibration, the correct determination of the particle rate and the effective spill duration.

The direct measurement with an ADC (having a gate of 150 ns) of the charge distribution of the mip signals through the front-end ("old Cardarelli" with voltage amplifier) gives a charge of the order of 1 pC at 2.9 kV (fig.26b). The evaluation of the total charge deposition per particle is not trivial because of the uncertainities due to the unknown front-end behaviour for signal with multi-cluster peaks and the small ADC gate used.

A P-Spice simulation of the full system TGC + Front-end has been performed for the prototype B which is equipped with the Sony charge preamplifier. Also in this case significantly smaller values of the charge per mip have been obtained, but the pre-amplifier integrates the charge for a short time (linear answer only up to 16 ns) so that the result is affected by very large uncertainties being almost insensitive to the clusters arriving with a large delay after the first one.

In the ATLAS muon TDR for the same chamber (same elementary cell and same gas mixture) a value of charge per mip corresponding to about 5 pC at 2.9 kV (about 2 times smaller than our first evaluation) is reported.

6.5 High rate performance

Fig.23 shows the TGC efficiency as a function of the particle rate per cm^2, measured at the SPS for a single gap of prototype A. All the points have been taken at an operating voltage of 3.2 kV. The efficiency remains of the order of 99% up to 30 kHz/cm^2 and decreases down to 95% at 200 kHz/cm^2. Similar measurements have been done during the PS test beam on prototype B. Fig.25 shows the efficiency of a single gap wire, pad and strip at various rates at an operating voltage of 3.0 kV. In the case of wire the efficiency remains >99% up to 50 kHz/cm^2 and slowly decreases at 98% at about 100 kHz/cm^2. This efficiency loss is not due to chamber inefficiency but can be fully explained by the dead time introduced by the front-end electronics. In fact, due to the large beam profile and the dimension of the group of wires connected to one front end channel, the input rate of the preamplifier is of the order of 300–400 kHz and the electronics dead time, calculated by the simulation, is about 50 ns and a tail increasing the threshold is cancelled in about 150 ns (see fig.24). We notice that such a rate should be an upper limit in the experiment.

The worse behaviour of the strips is explained by the position of the operating voltage (3.0 kV) at the knee of the strip plateau. The voltage drop which has no effect for wire and pads, produces a loss of efficiency on the strips of the order of ~6% in addition to the front-end dead time. This effect of voltage drop can be reduced with a better connection graphite ground.

The effect of voltage drop is easily reproduced by simulation. Considering a connection graphite-ground all along the 80 cm sides of the chamber and a graphite resistivity of 200 kΩ/sq, and assuming a charge deposition of 10 pC per particle a voltage drop of 16 V is obtained at a particle rate of 100 kHz/cm^2 over the full chamber area.

Fig.25 shows the cluster size as a function of the particle rate. At rate up to 150 kHz/cm^2 no variations of the cluster size are present.

In conclusion TGC chambers equipped with the Sony ASD do not show any performance limitation due to rate.

7 Ageing

The TGC are normally operated at high gain, nevertheless they are expected to be relatively radiation resistant. Due to the use of a highly quenching gas, there is only a very small dependence of the charge on the particle incident angle, and no streamers and no special events with very large charge multiplication are expected.

The wires have a relatively large diameter of 50 μm. The graphite layer is known to behave better than copper conductive cathodes, being more inert to charge deposition and the variations in graphite resistivity (that have been observed in detectors subjected to high radiation doses) have only a small effect on the signal induced in the conductive electrodes.

The ageing problems are essentially concentrated on the wires and we may assume as significant the existing ageing tests performed by the ATLAS collaboration with a local irradiation.

7.1 ATLAS ageing tests

The ATLAS ageing measurements were done on chambers having the same characteristics (elementary cell and gas mixture) of the chambers we are testing. The test was performed operating the chambers at 3.2 kV; in these conditions the gas gain is more than 2 times higher than the gas gain of a chamber operating at 2.9 kV (see fig.26b), which is for us a reasonable working point.

Four 10×10 cm^2 TGC have been irradiated with a ^{90}Sr source. The size of the irradiated area was about 1 cm^2 FWHM. The response of the chambers for various gas flow rates was monitored, triggering on beta particles traversing the chamber. The pulse charge measured with an ADC, the time jitter (arrival time of the first avalanche) and the chamber current were recorded.

No change in performance has been observed in a chamber subjected to irradiation at a rate of 200 kHz/cm^2 for over 1000 hours (see fig. Atlas). Considering an LHC effective year of 10^7 s and a chamber operating at 2.9 kV, this dose corresponds to a life time of >10 years at 16 kHz, a dose which is significantly larger than the expected dose in the inner regions of the stations M2–M5.

We can conclude that no strong ageing problems are expected for the chambers M2–M5 So for these chambers we propose to operate with wires chambers making use of a highly quenching and relatively high gain gas mixture which has several positive features and in particular permits to work easily with the well known and not expensive Sony chip. On the other hand, taking into account that the Atlas test is a test of local irradiation, one should look more carefully to the situation in the inner regions, possibly operating TGC at lower gain. For M1 station a different solution has to be studied : different gas mixture, different chamber parameters and different electronic front-end.

8 Simulation

The detector simulation is well under control and is proceeding in 3 streams:

- Garfield: Chamber cell and gas simulation
- P-spice electronic model of the TGCchamber and front-end simulation
- SICB Monte Carlo Simulation of the layout and the time effects to compute the trigger efficiency.

  The time spread of the signals from logical channels has been simulated taking into account several effects and their influence on the trigger performance.

9 Construction procedure

The chamber design and the construction procedure has been studied for a long time at the Rehovot Weizmann Institute in Israel and is now wery well established.

Two single-gap chambers are built at the same time. Four half shells are prepared : Each shell is composed of a G10 layer 1.6 mm thick and a frame of G10, 1.4 mm thick. The G10 layer has graphite varnish on one side (with an external conductive strip in contact with the 1.4 mm thick frame) and the copper cathode electrodes on the other side. Spacers can be added in case of large size chambers. Two of the four shells are put on the two sides of a rotating table which is supplied with a vacuum system to fix the shells. The two half chambers are simultaneously wired, the wires are soldered and cut and the two half chambers are glued with the corresponding half shells.

The design and construction procedure of TGCs is wery well tested and It has been easily extended to produce double gap chambers with different requirements of wire- or size and shape of conductive cathode electrodes. The procedure essentially doesn't change for the production of pad or strip chambers and is well tested for chambers of the dimension required by the proposed layout.

Mechanical constructive details are available.

The chambers' shells can be industrially prepared (contacts with DITRON Italy)

There is the need of a Laboratory for chamber wiring and gluing.

10 Costs

Preliminary cost evaluation ($\pm$ 20%) is done for 1 bigap layer everywhere.

Regions R1 + R2:	
96 bigap chambers $\sim$ 30 m^2 hi-tech board (4 layers)	110 KSF
covers (2layers)	4 KSF
HV conn. 240 x 10	2.4 KSF
Gas conn. 240 x 5	1.2 KSF
Extra (wire, spacers,etc)	10 KSF
TOTAL	130 KSF
+ Manpower 0.4 y x 10 men	

Regions R3 + R4:	
240 bigap chambers 210 sheets x 6 x 150 SF	190 KSF
HV conn 480 x 10	4.8 KSF
Gas conn. 480 x 5	2.4 KSF
Extra (honeycomb, wire,..)	20 KSF
TOTAL	220 KSF
+ Manpower 1.0 y x 10 men	

TOOLING:	
wiring machine	80 - 100 KSF
varnishing machine	20 KSF
reference tables	40 - 50 KSF
vac pumps, air compr.	30 KSF
extra (infrastructures)	50 - 100 KSF
TOTAL	210 - 400 KSF

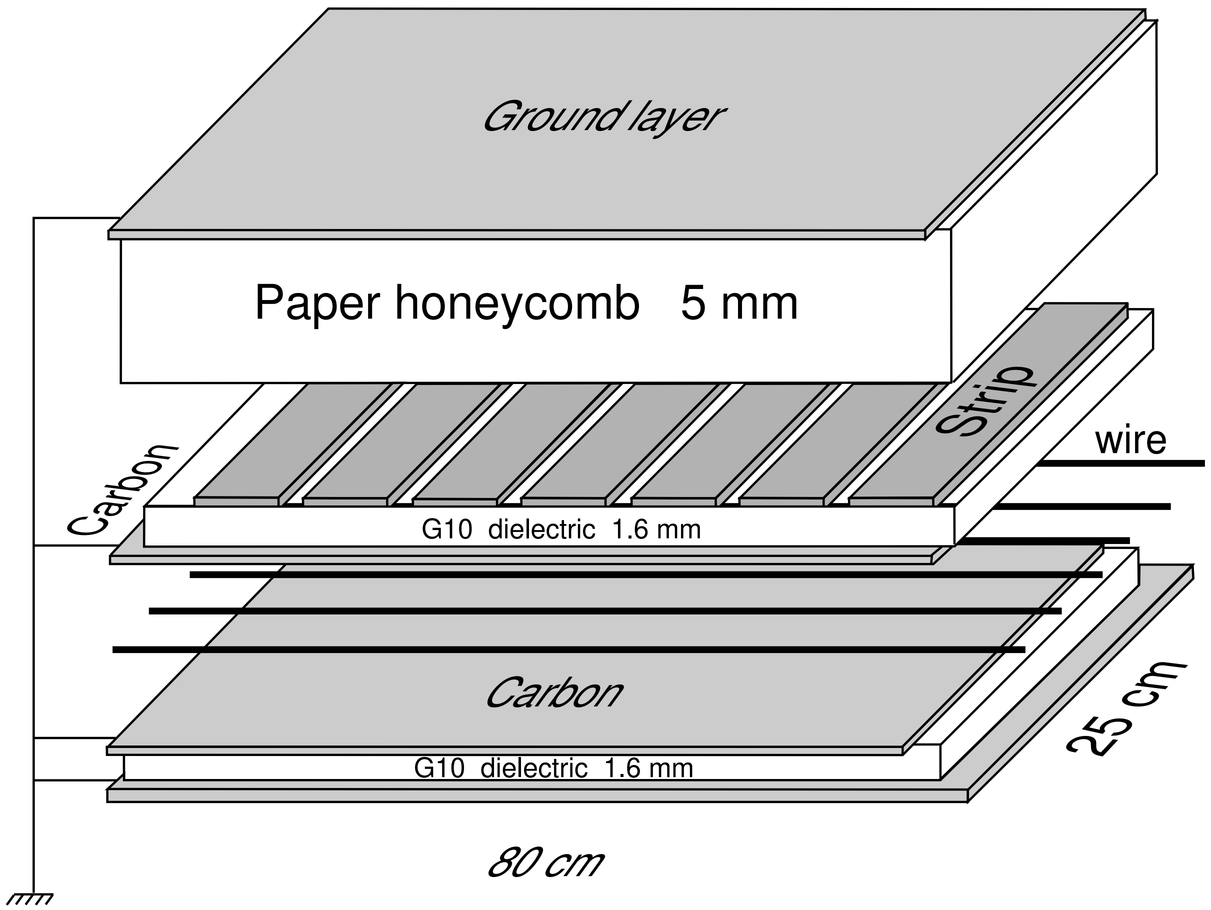


Figure 1: Schematic view of a TGC.

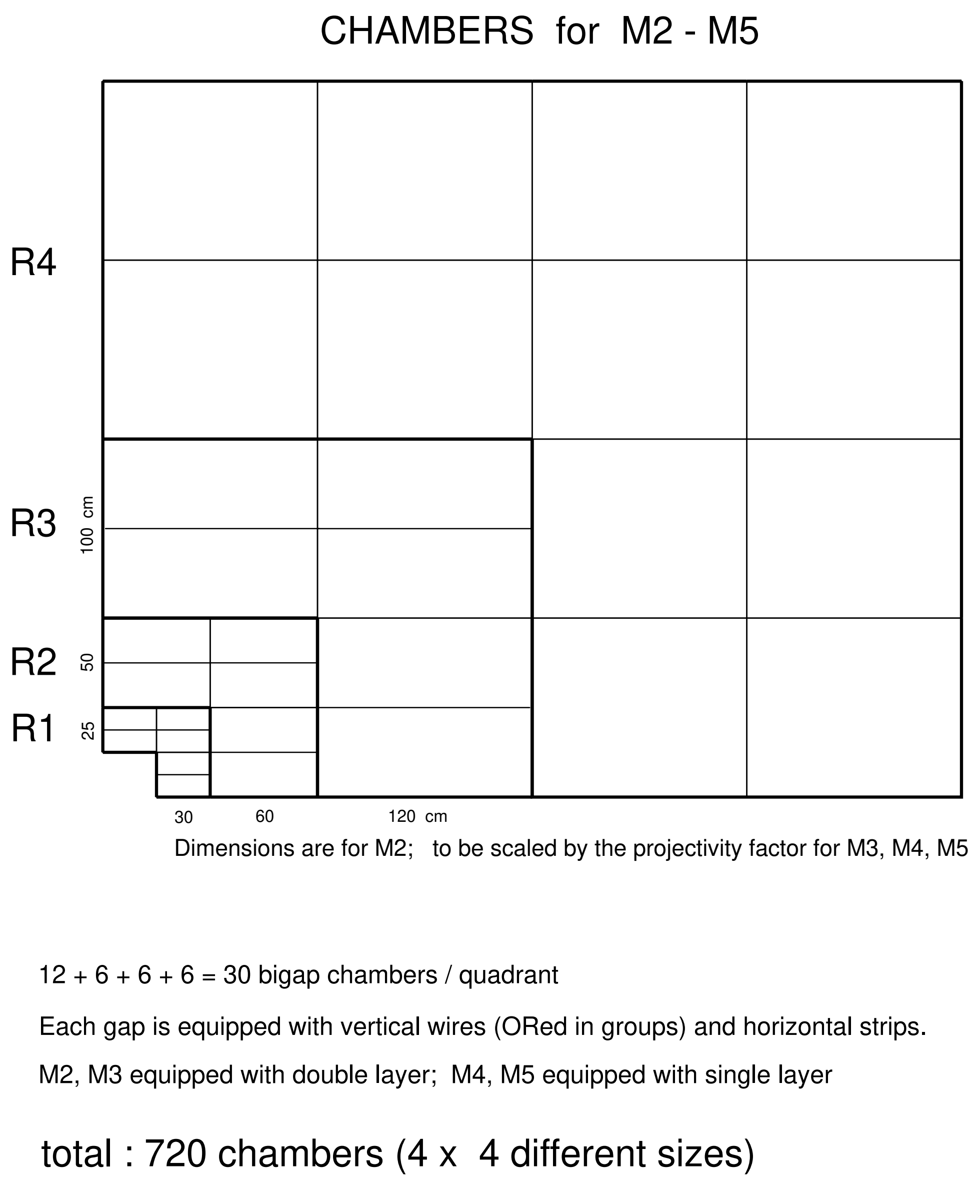
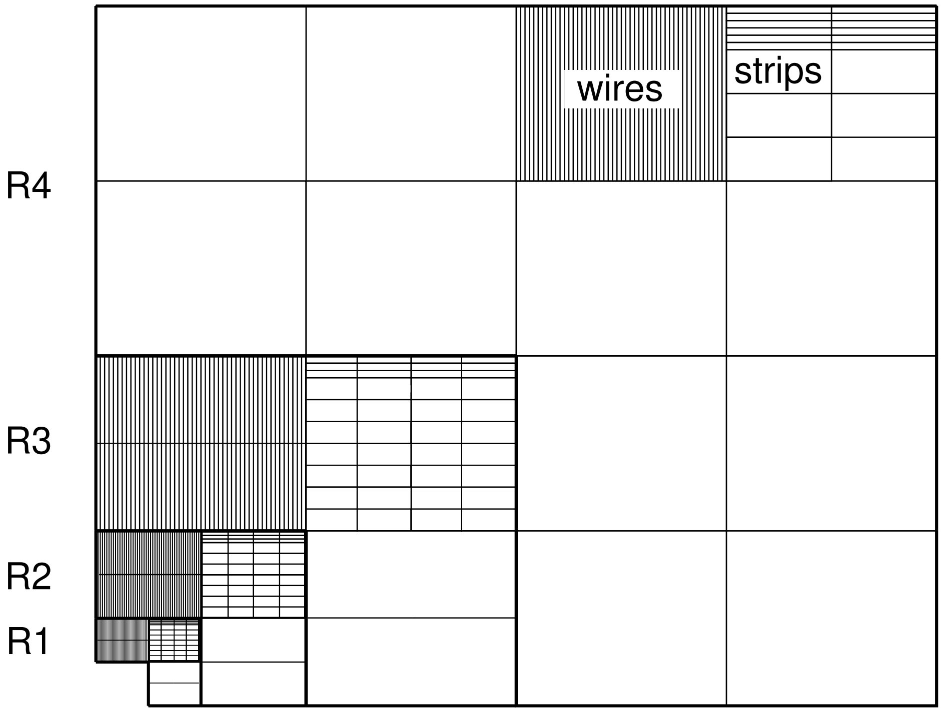


Figure 2: Chambers' layout.

PHYSICAL WIRES AND STRIPS for M2 - M5



The dimensions are for M2

	WIRE GROUPS / chamber			STRIPS / chamber	
	number	dimensions (cm)	max. rate (kHz)	number	dimenions (cm)
region R1:	48	0.63 x 12.5	37	48	7.5 x 1
region R2:	48	1.25 x 25	75	48	15 x 2.1
region R3:	48	2.5 x 50	100	48	30 x 4.2
region R4:	48	2.5 x 100	25	48	60 x 4.2
		(160-200 pF)			(60-70 pF)

CHANNELS / quadrant

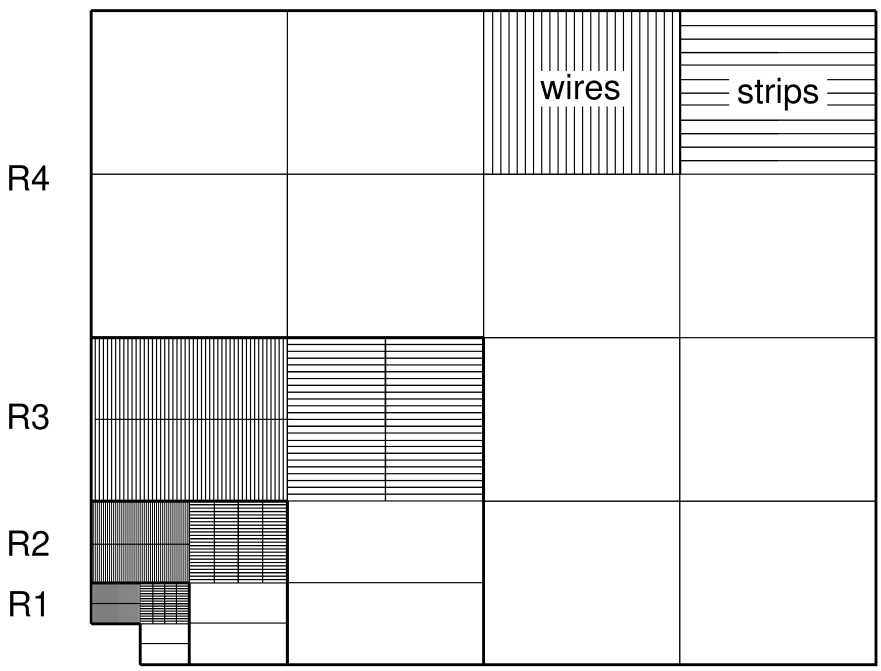
	wires	strips
region R1:	288	288
region R2:	288	288
region R3:	288	288
region R4:	576	576
total :	1440	1440

TOTAL # CHANNELS

69120 with 1 front-end /bigap
or
138240 with 1 front-end /gap

Figure 3: Physical channels.

LOGICAL WIRES AND STRIPS for M2, M3



The dimensions are for M2

	WIRES / chamber number	dimensions (cm)	max. occup. (%)	STRIPS / chamber number	dimensions (cm)	max. occup. (%)
region R1:	48	0.63 x 12.5	2.0	48	7.5 x 1.	2.0
region R2:	48	1.25 x 25	1.5	48	15 x 2.1	3.0
region R3:	48	2.5 x 50	0.8	24	60 x 4.2	1.6
region R4:	24	5 x 100	0.4	12	120 x 8.3	0.8

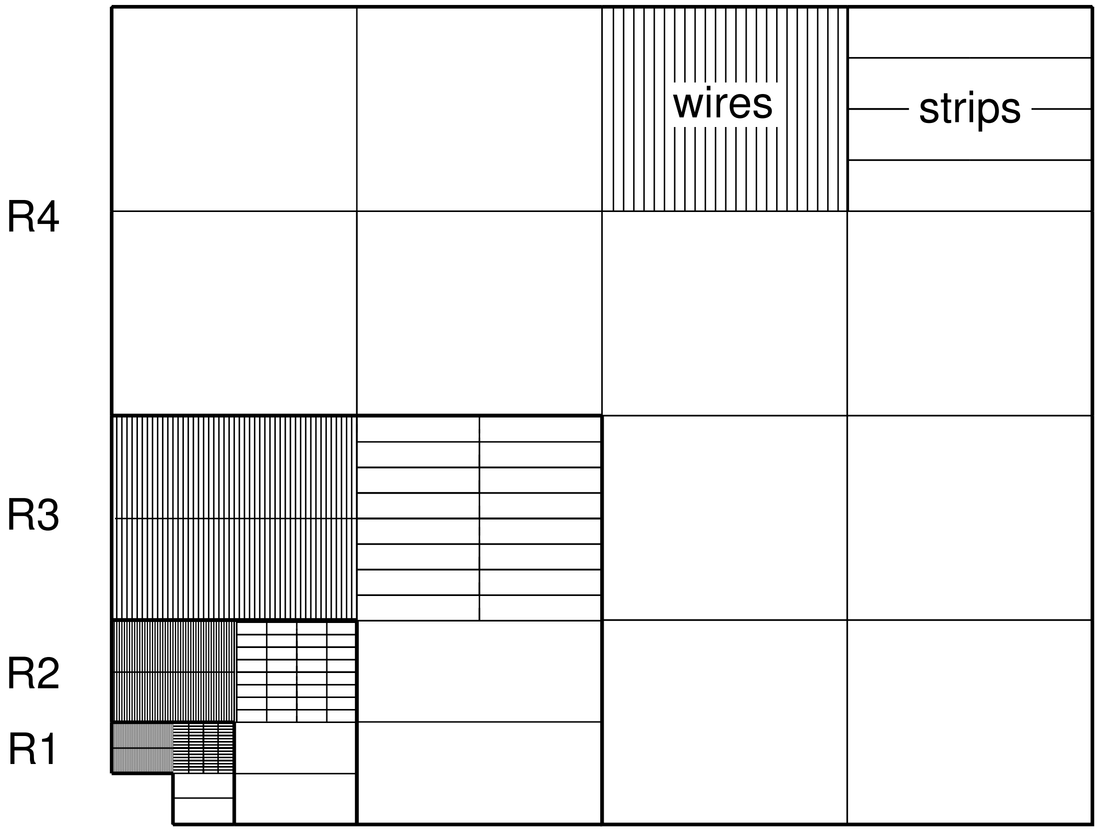
CHANNELS / quadrant

	wires	strips
region R1:	288	288
region R2:	288	288
region R3:	288	144
region R4:	288	144
total :	1152	864

TOTAL # CHANNELS
8064 + 8064 for M2 + M3

Figure 4: M2-M3 logical channels.

LOGICAL WIRES AND STRIPS for M4, M5



The dimensions are for M5

	WIRES / chamber			STRIPS / chamber		
	number	dimensions (cm)	max. occup. (%)	number	dimensions (cm)	max. occup. (%)
region R1:	24	1.6 x 15	2.5	16	9.3 x 1.9	2.0
region R2:	12	6.3 x 31	0.4	16	18.7 x 7.8	1.0
region R3:	12	12.5 x 62	0.3	8	75 x 15.5	0.6
region R4:	6	25 x 124	0.4	4	150 x 31	0.8

CHANNELS / quadrant

	wires	strips
region R1:	144	96
region R2:	72	96
region R3:	72	48
region R4:	72	48
total :	360	288

TOTAL # CHANNELS

2592 + 2592 for M4 + M5

Figure 5: M4-M5 logical channels.

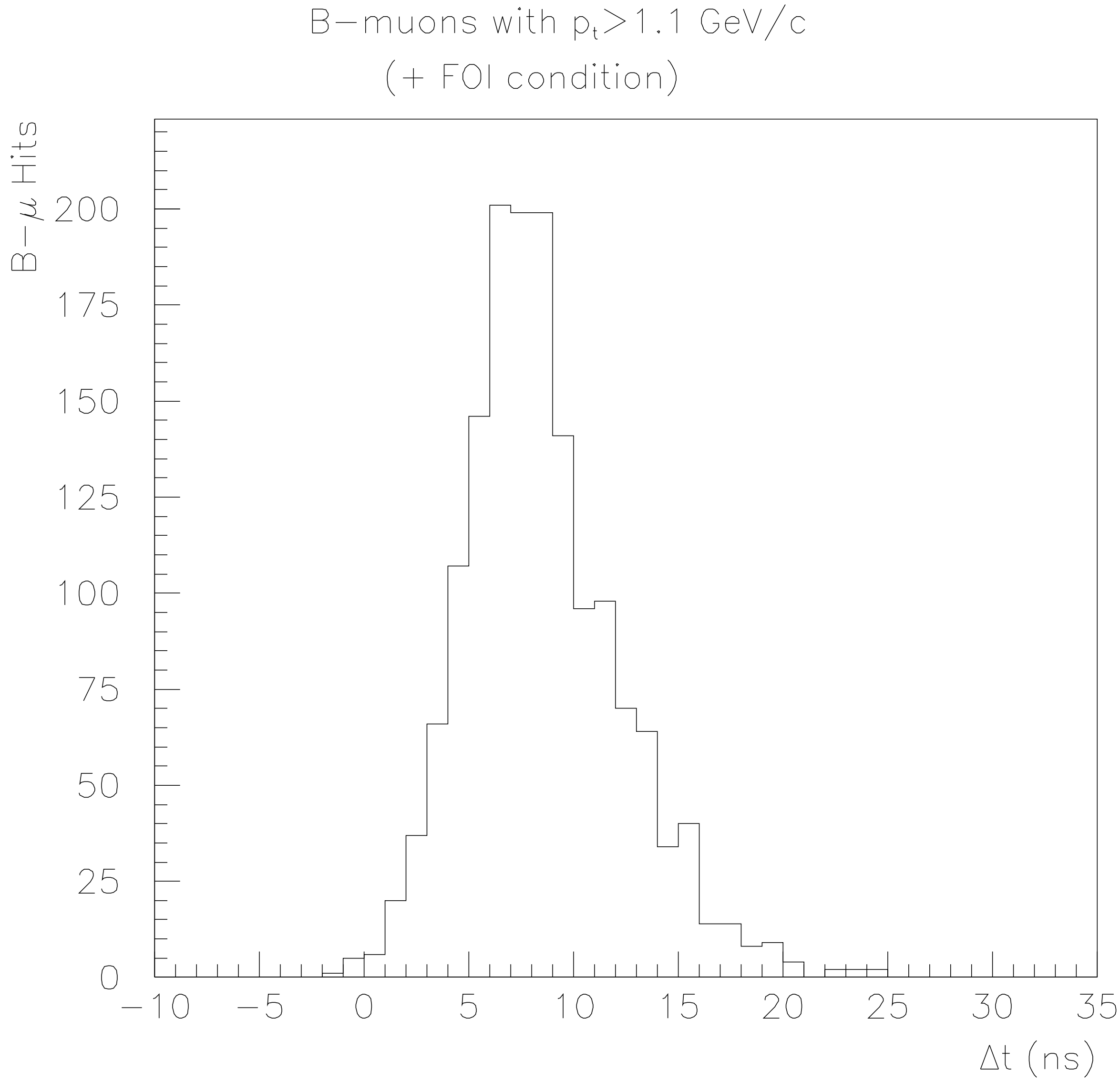


Figure 6: Simulated time distribution

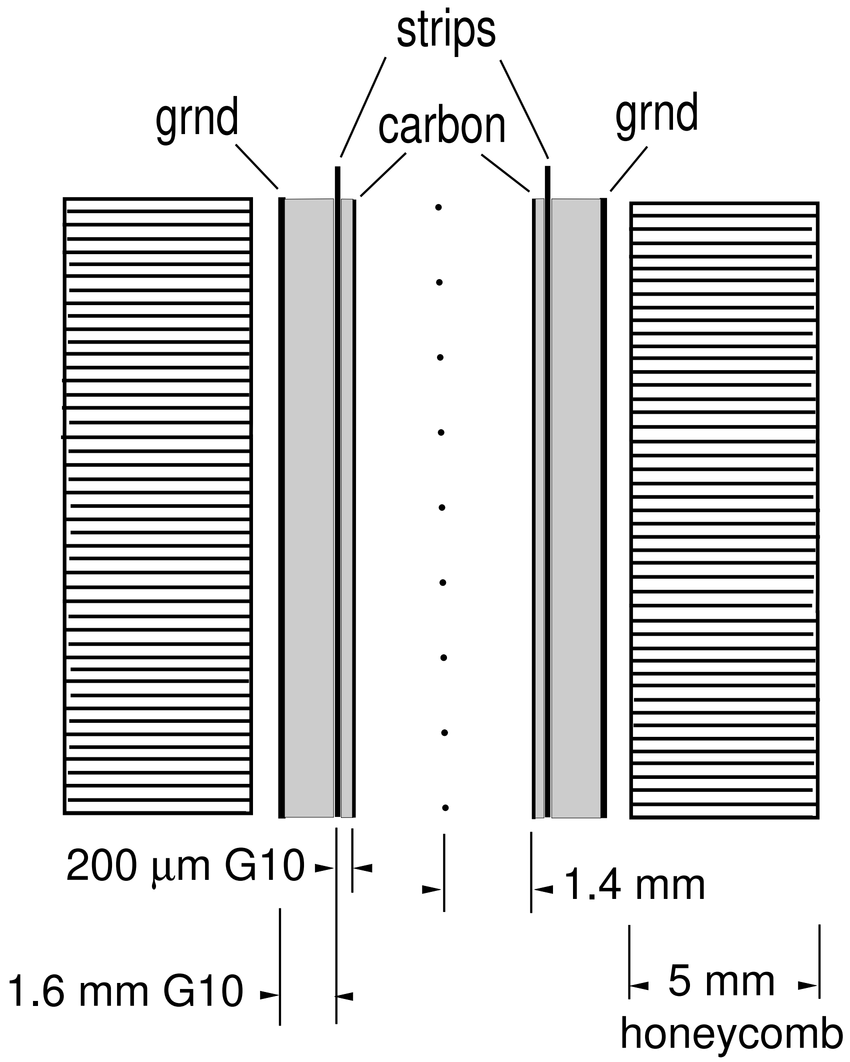


Figure 7: Prototype A

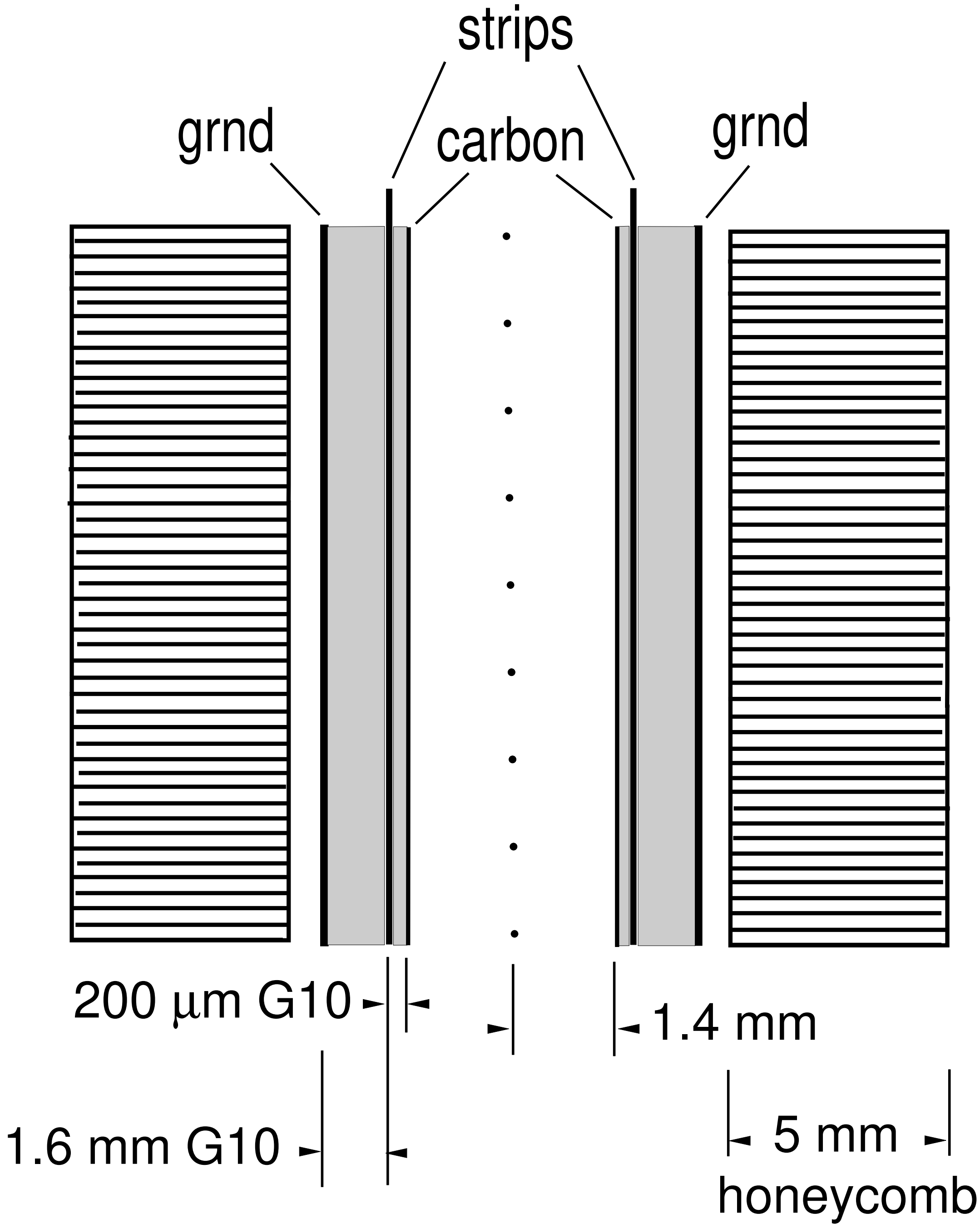


Figure 8: Prototype B

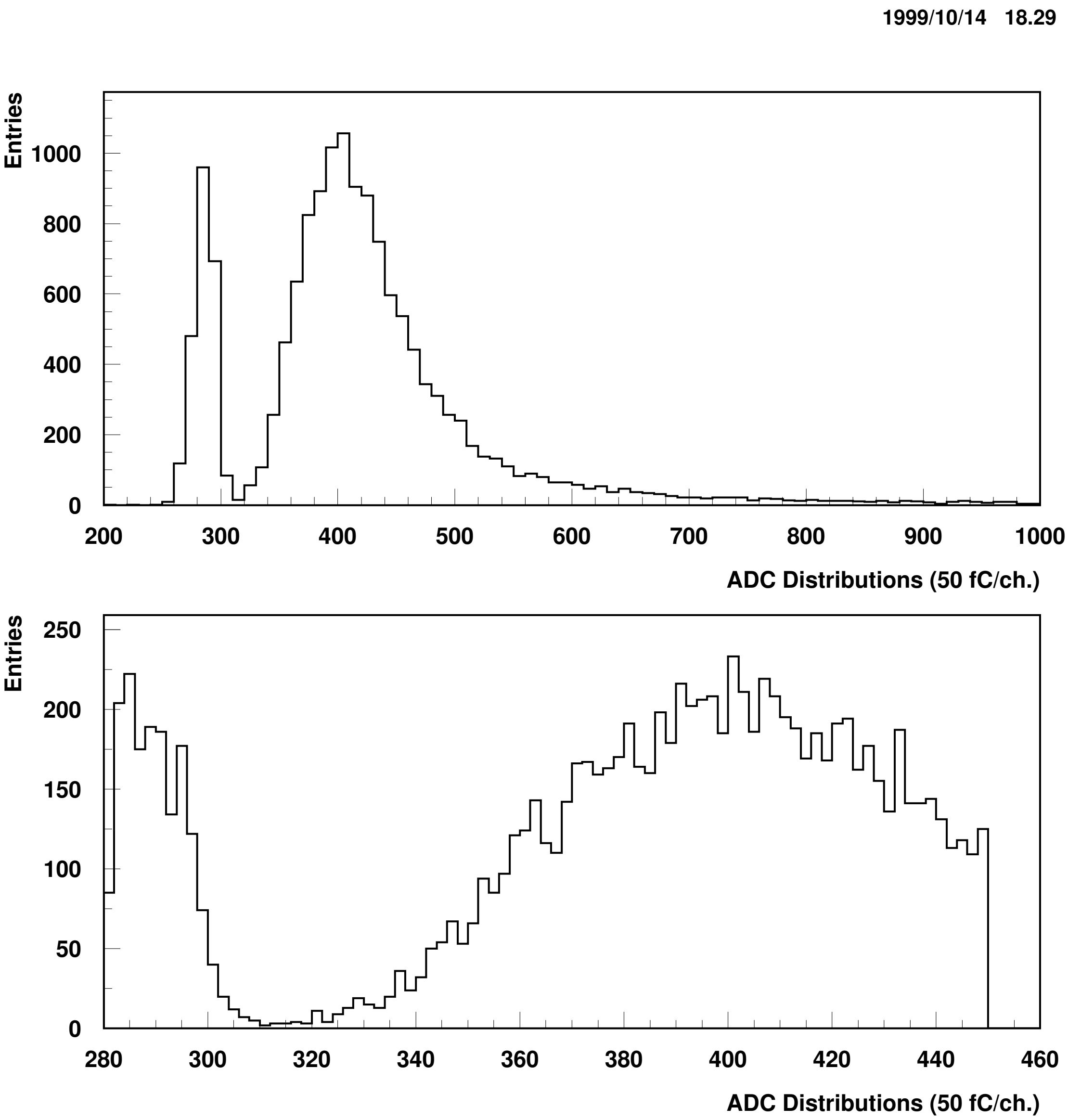


Figure 9: Wires ADC distribution.

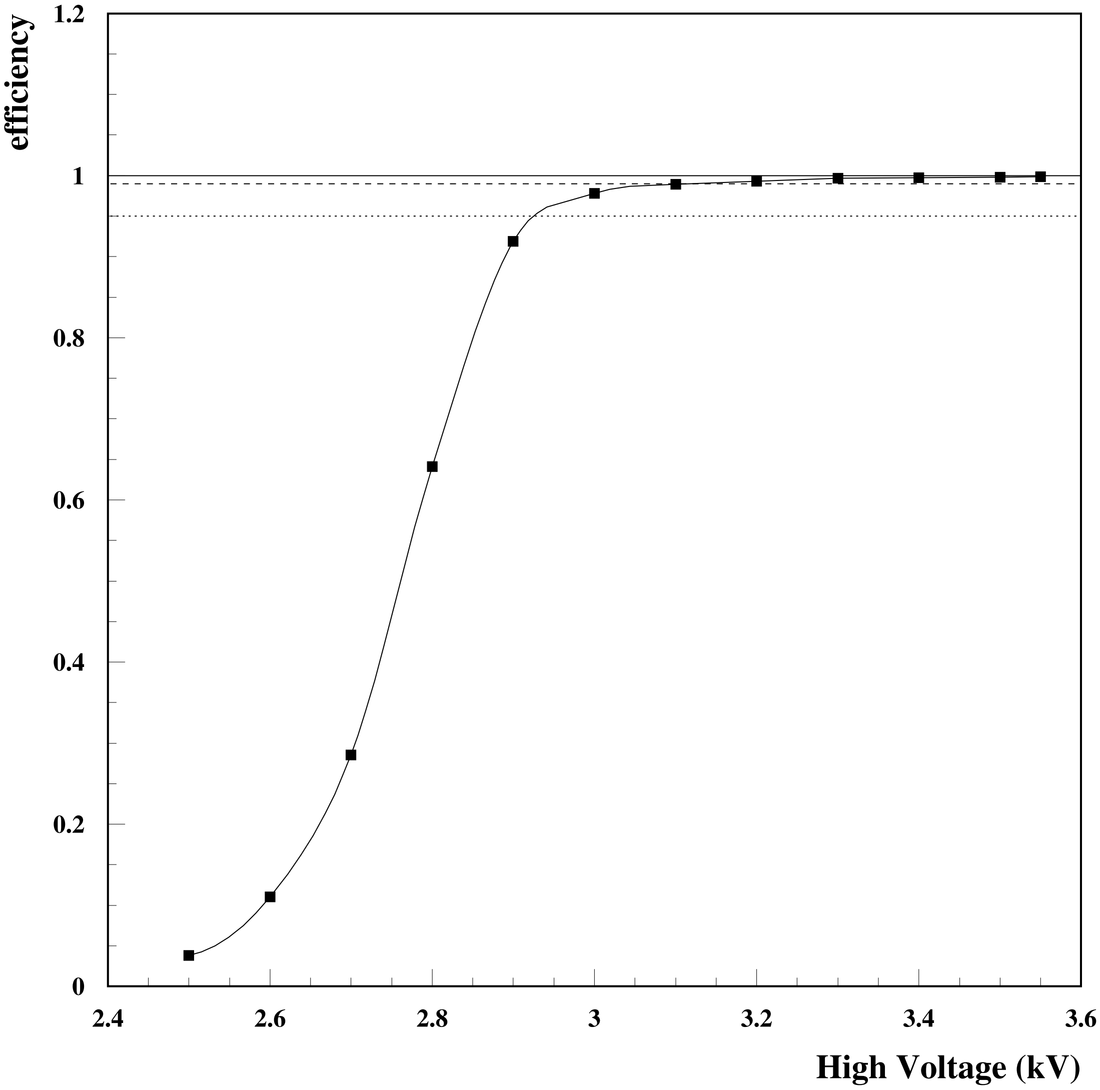


Figure 10: Wire efficiency for prototype A

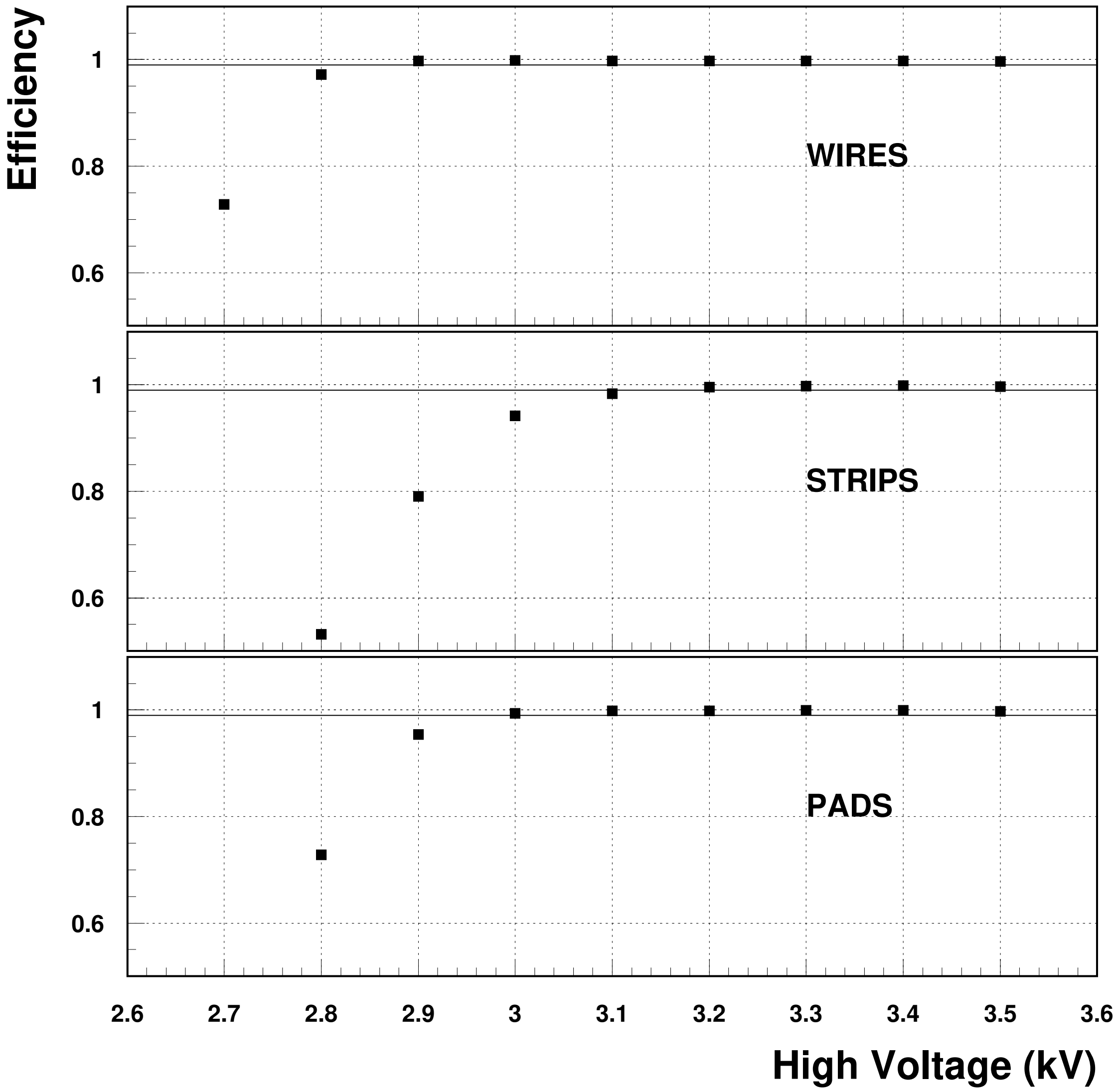


Figure 11: Efficiencies for prototype B

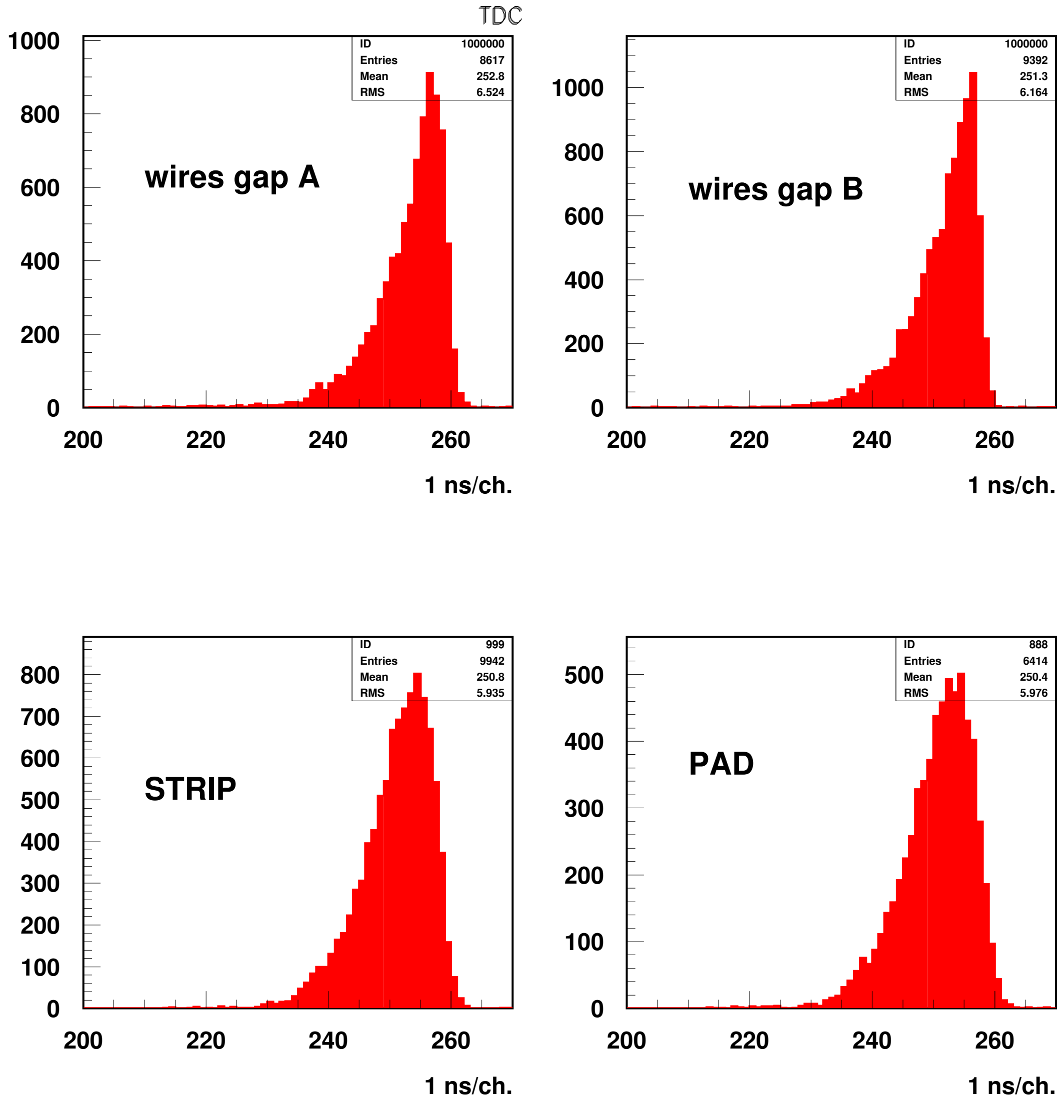


Figure 12: TDC distributions.

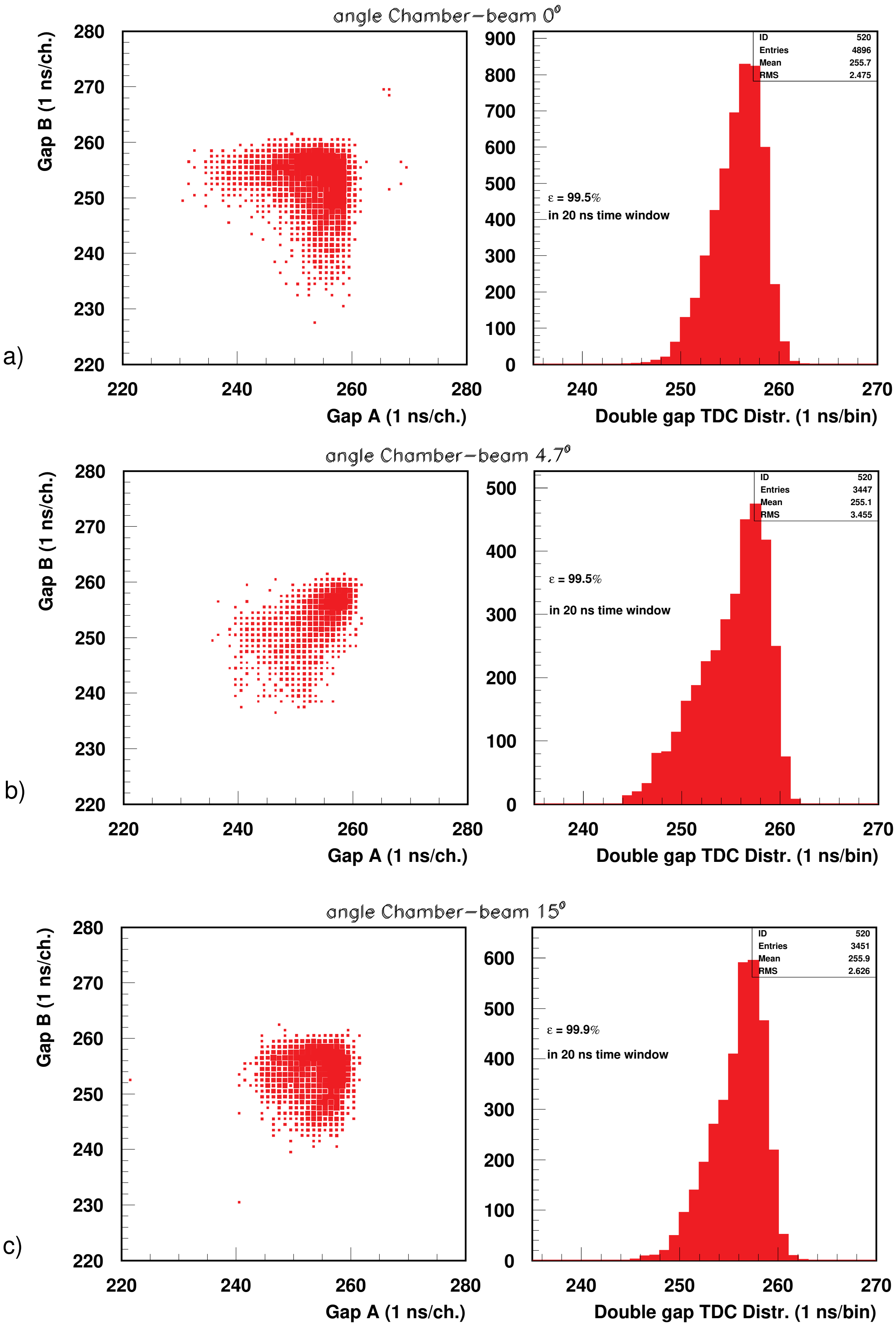


Figure 13: TDC distribution of ORed bigap at different tracks inclinations: a) 0° degrees, b) 4° degrees, c) 15° degrees.

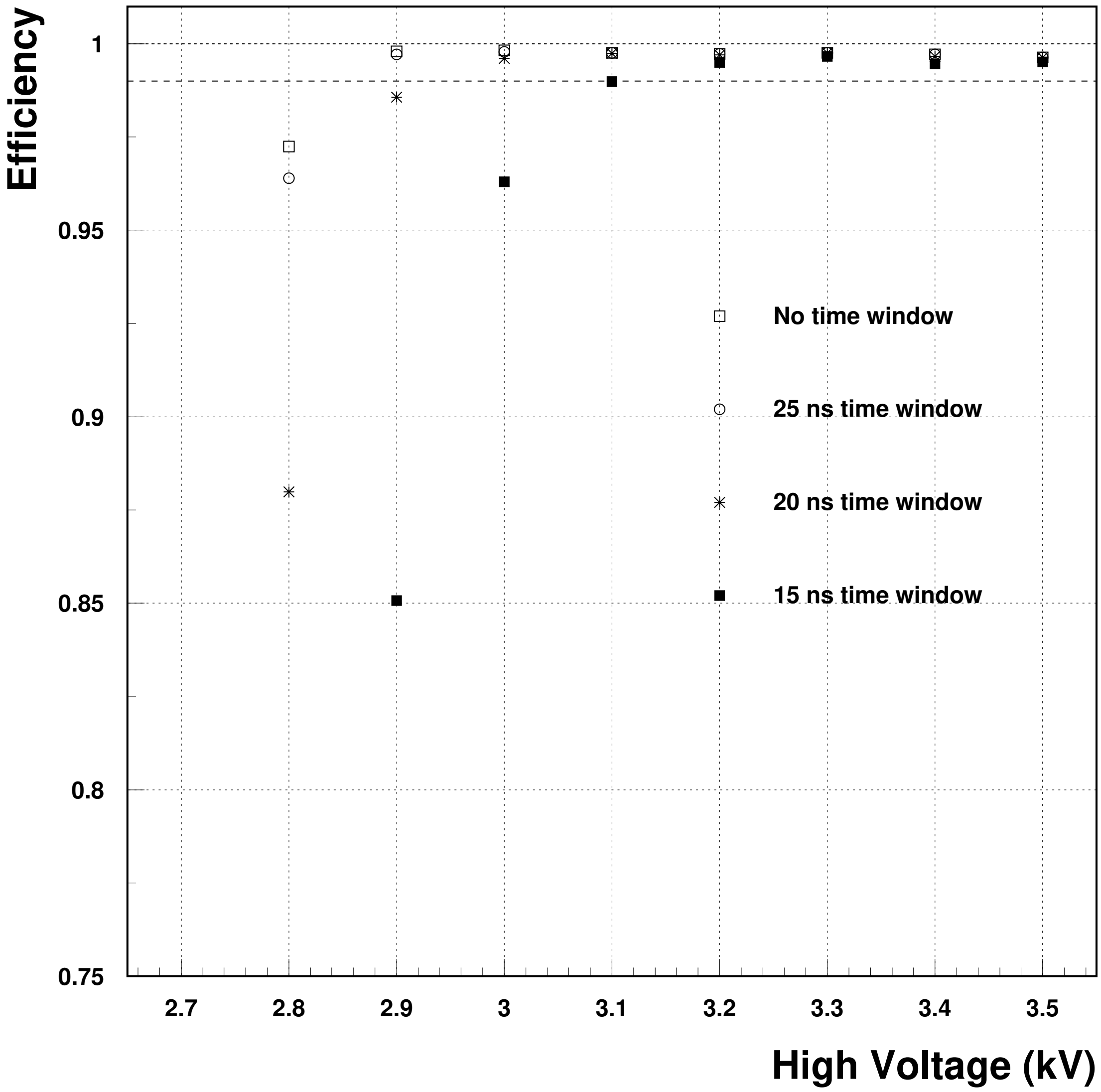


Figure 14: Efficiencies for the ORed wire for different time windows as functions of high voltage.

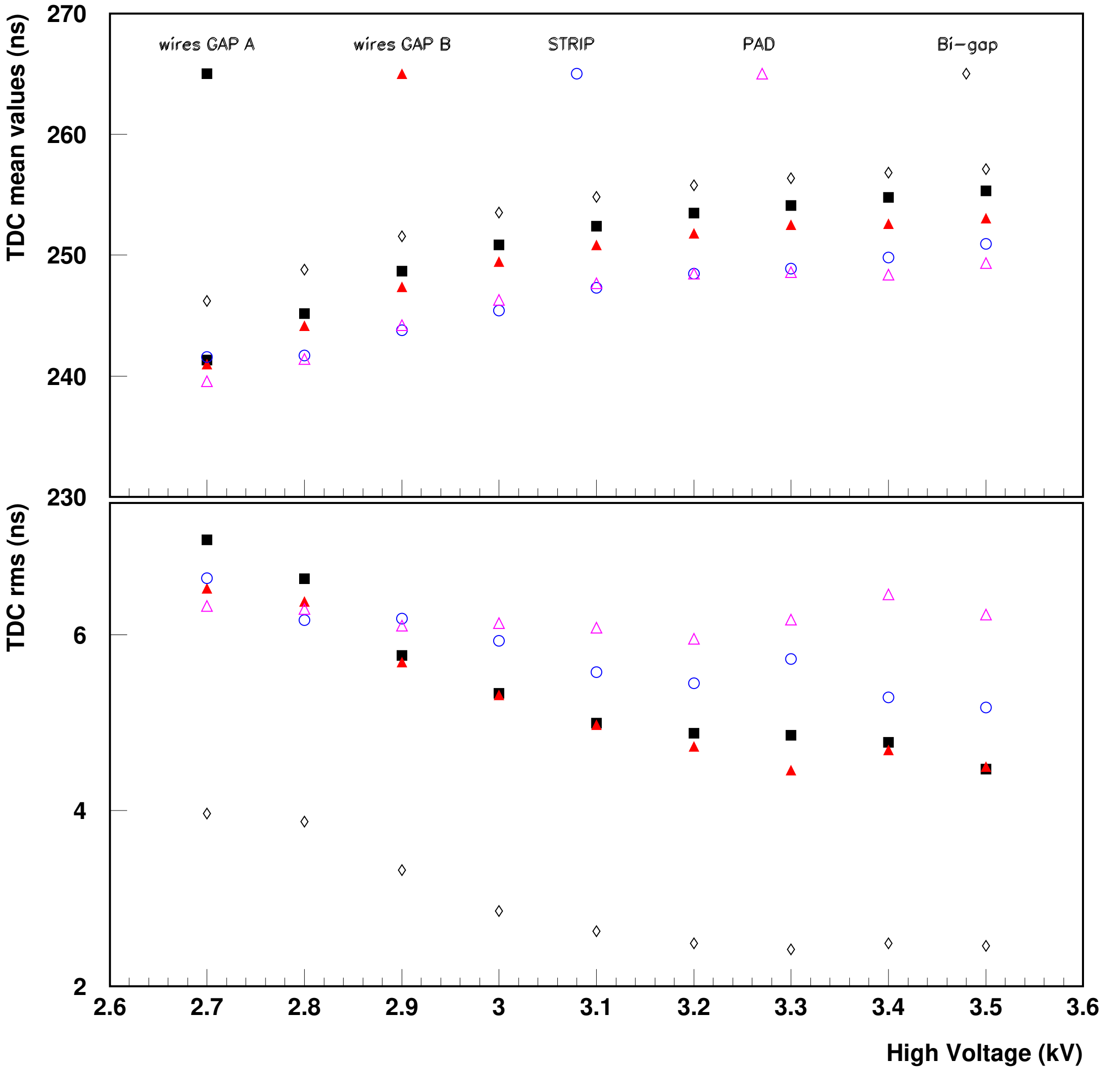


Figure 15: TDC mean value and R.M.S. as functions of high voltage.

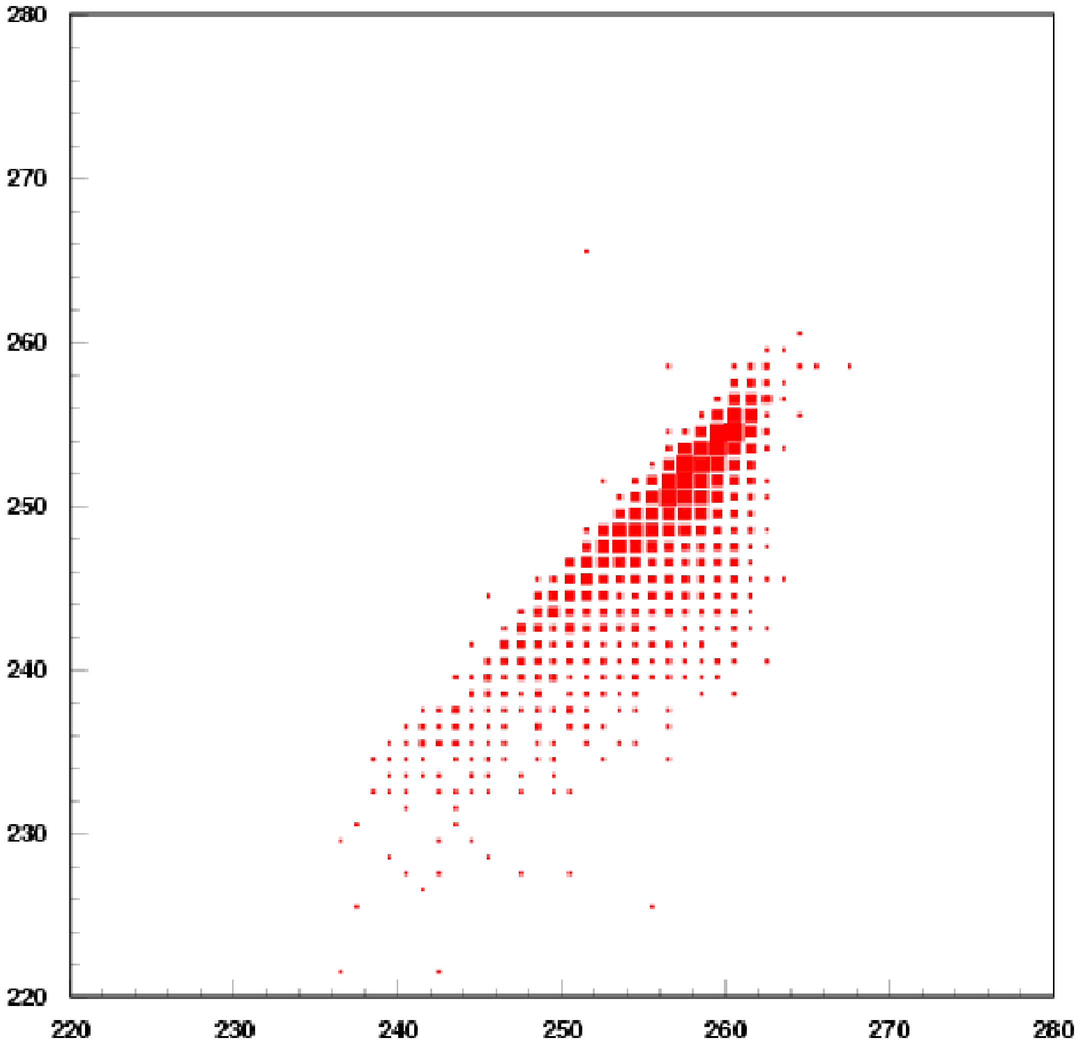


Figure 16: Wire TDC vs. strip TDC correlation.

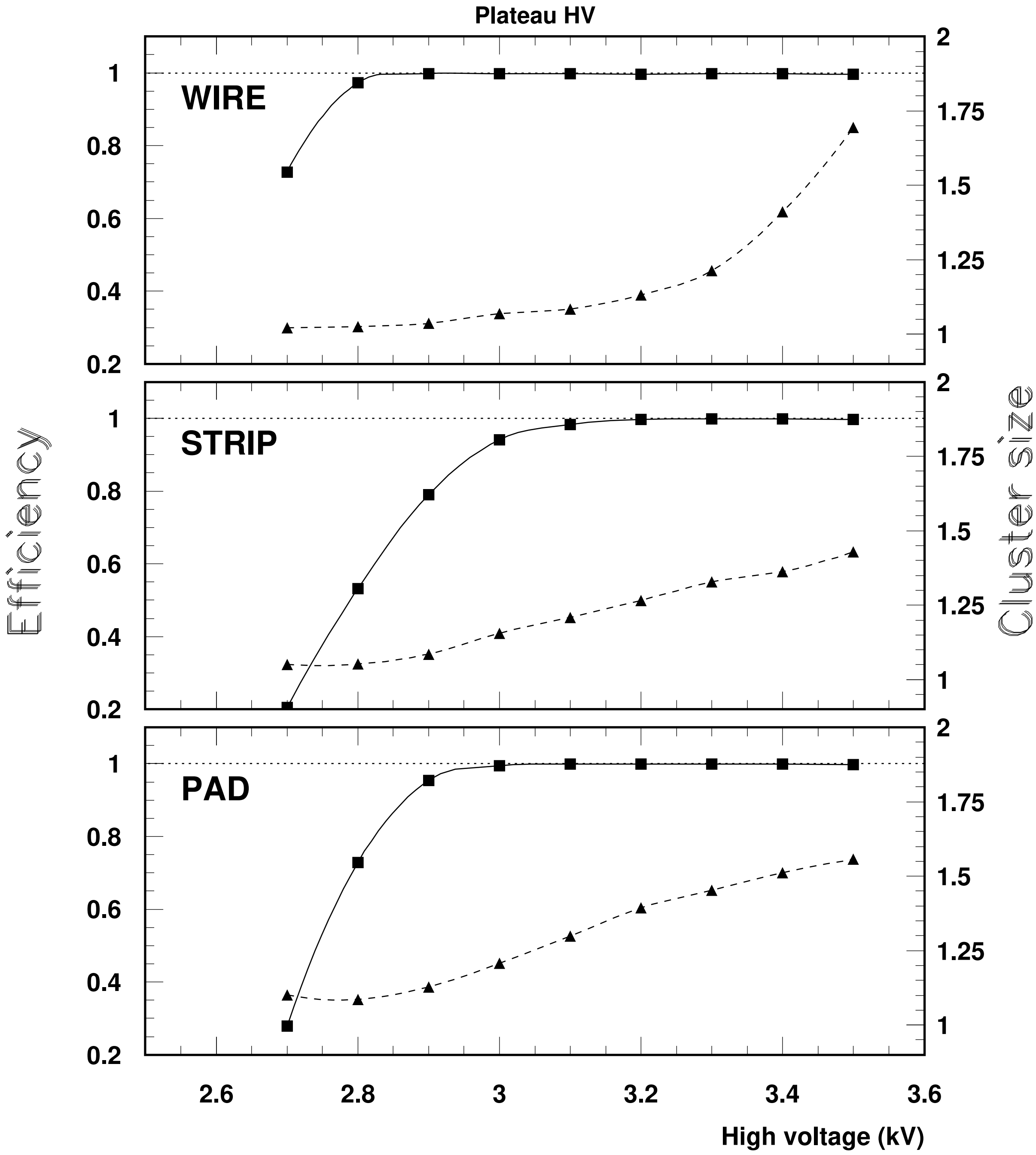


Figure 17: Cluster size vs. high voltage.

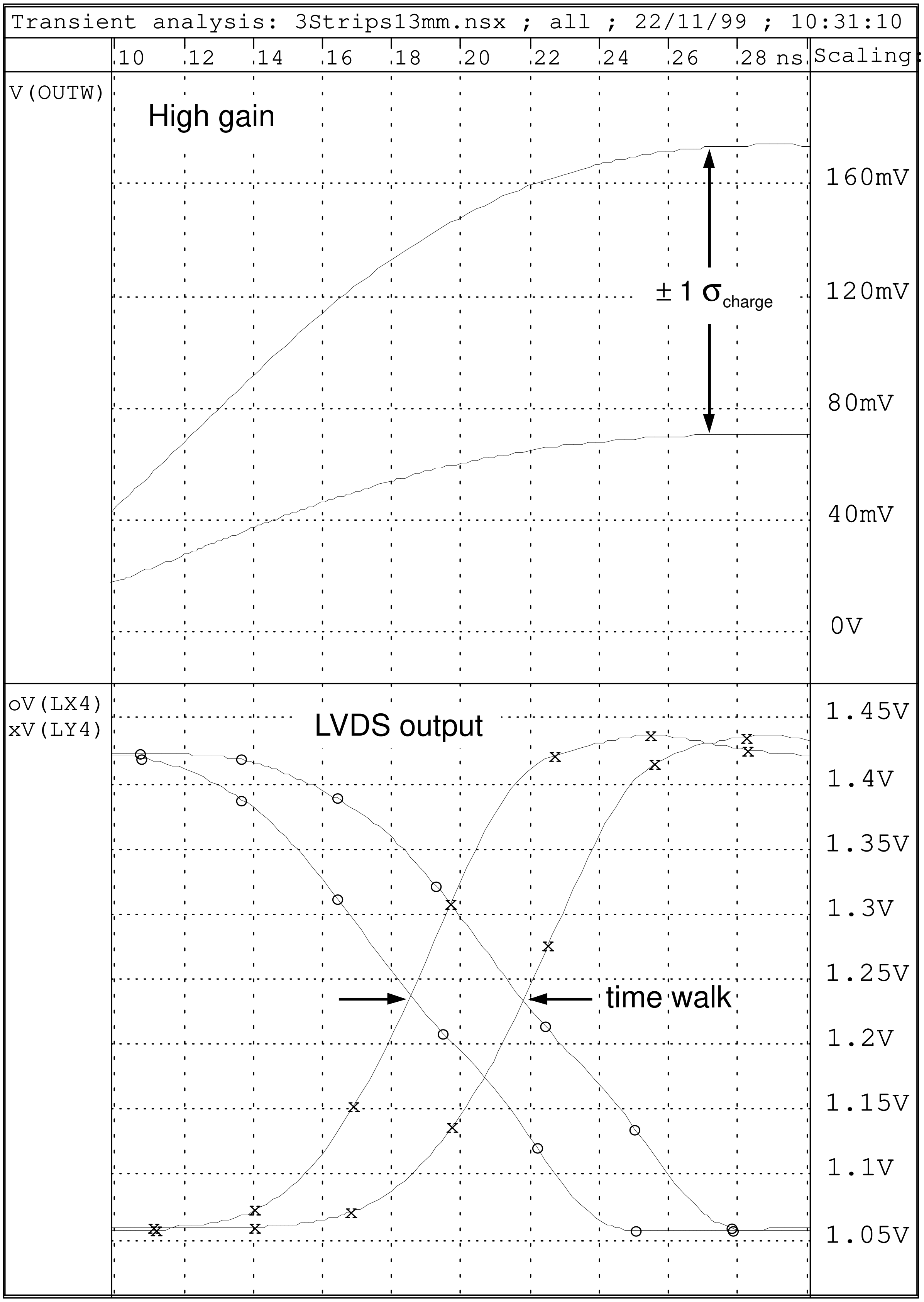


Figure 18: Simulated time walk for TGC operating at high gain. Threshold=-300mV as in the test of prototype B

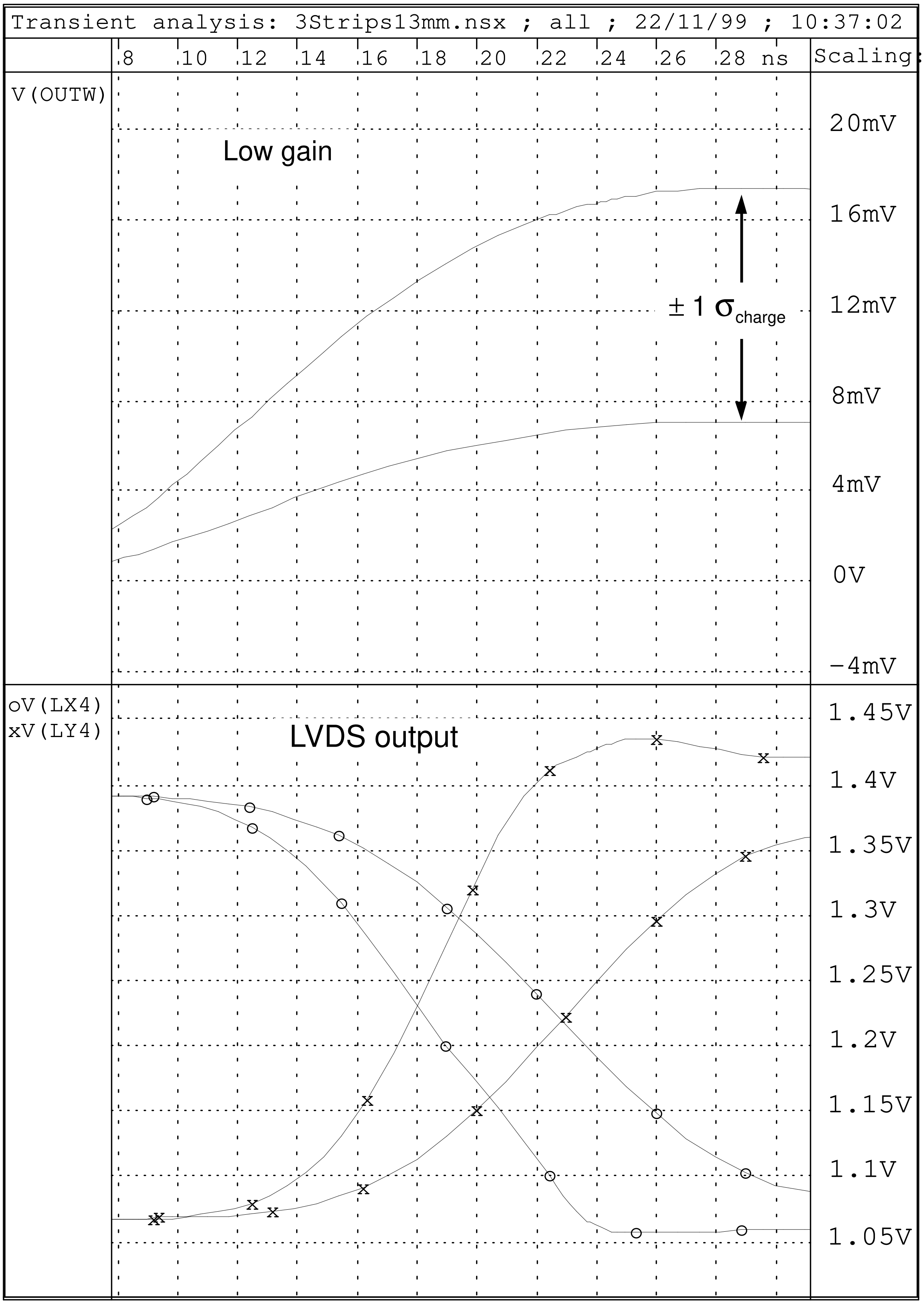


Figure 19: Simulated time walk for TGC operating at low gain. A very low threshold=-10mV has been used to obtain e reasonable time walk

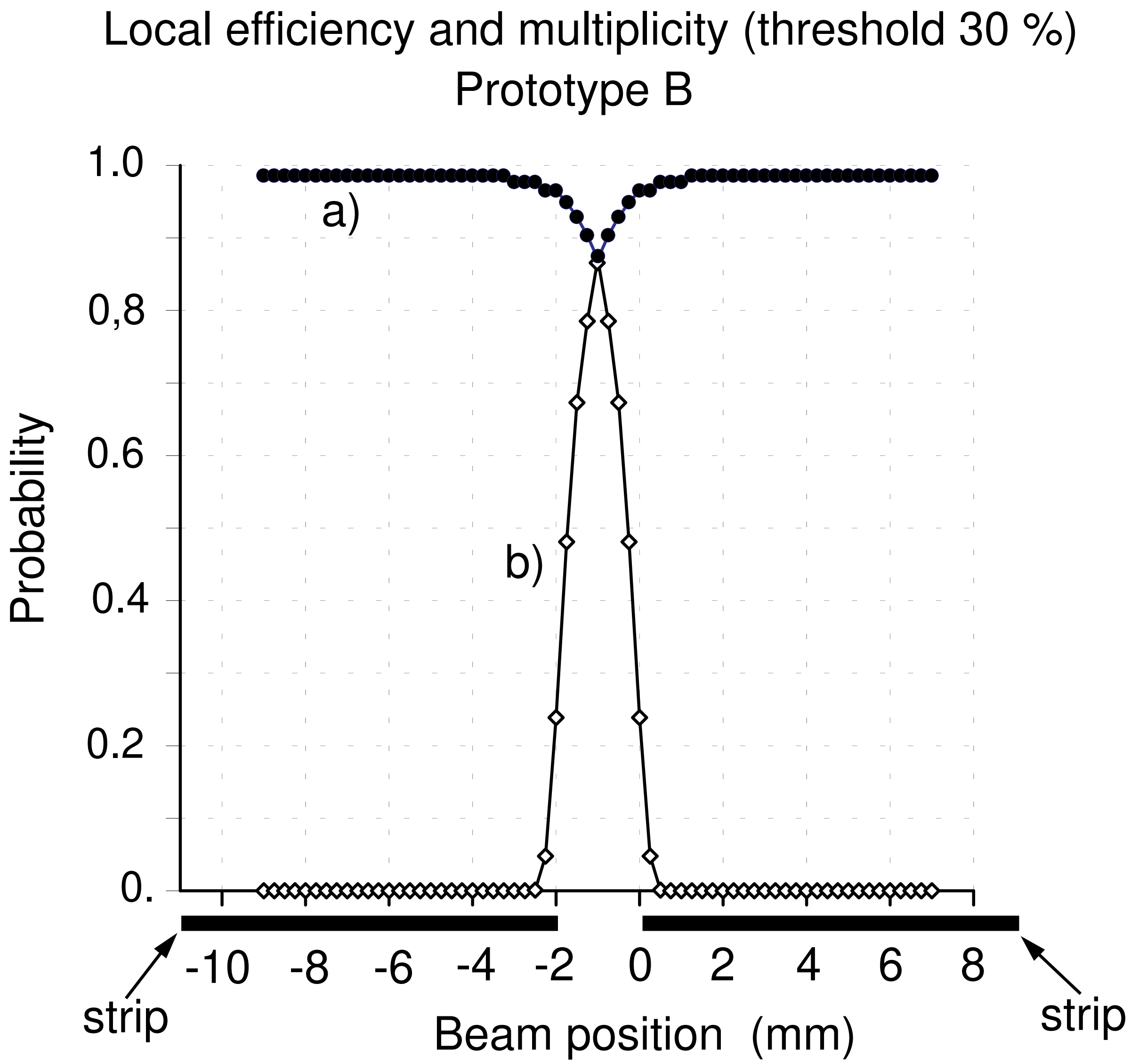


Figure 20: Simulation of a) efficiency and b) crosstalk vs. beam position.

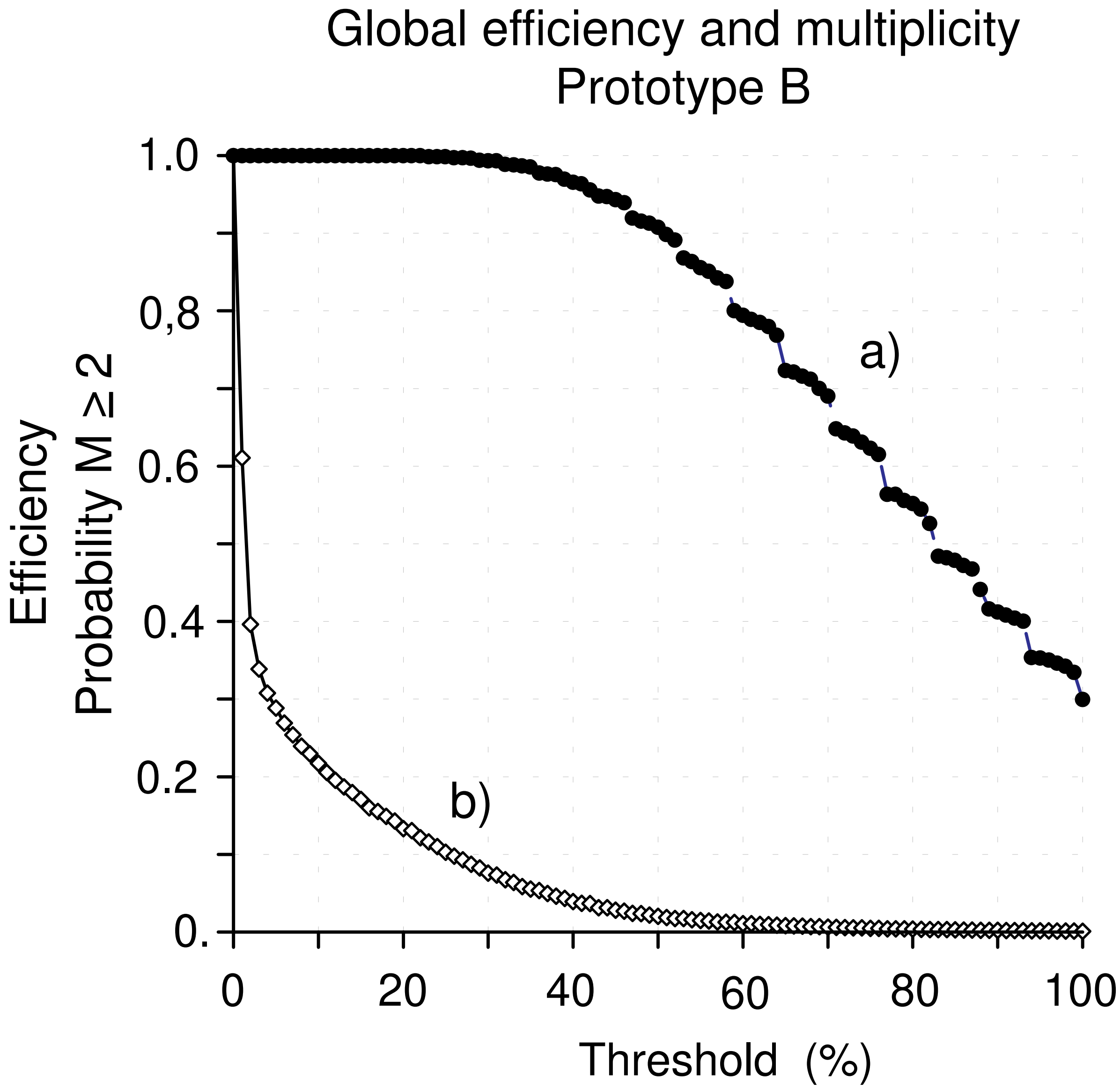


Figure 21: Simulation of a) efficiency and b) crosstalk vs. threshold.

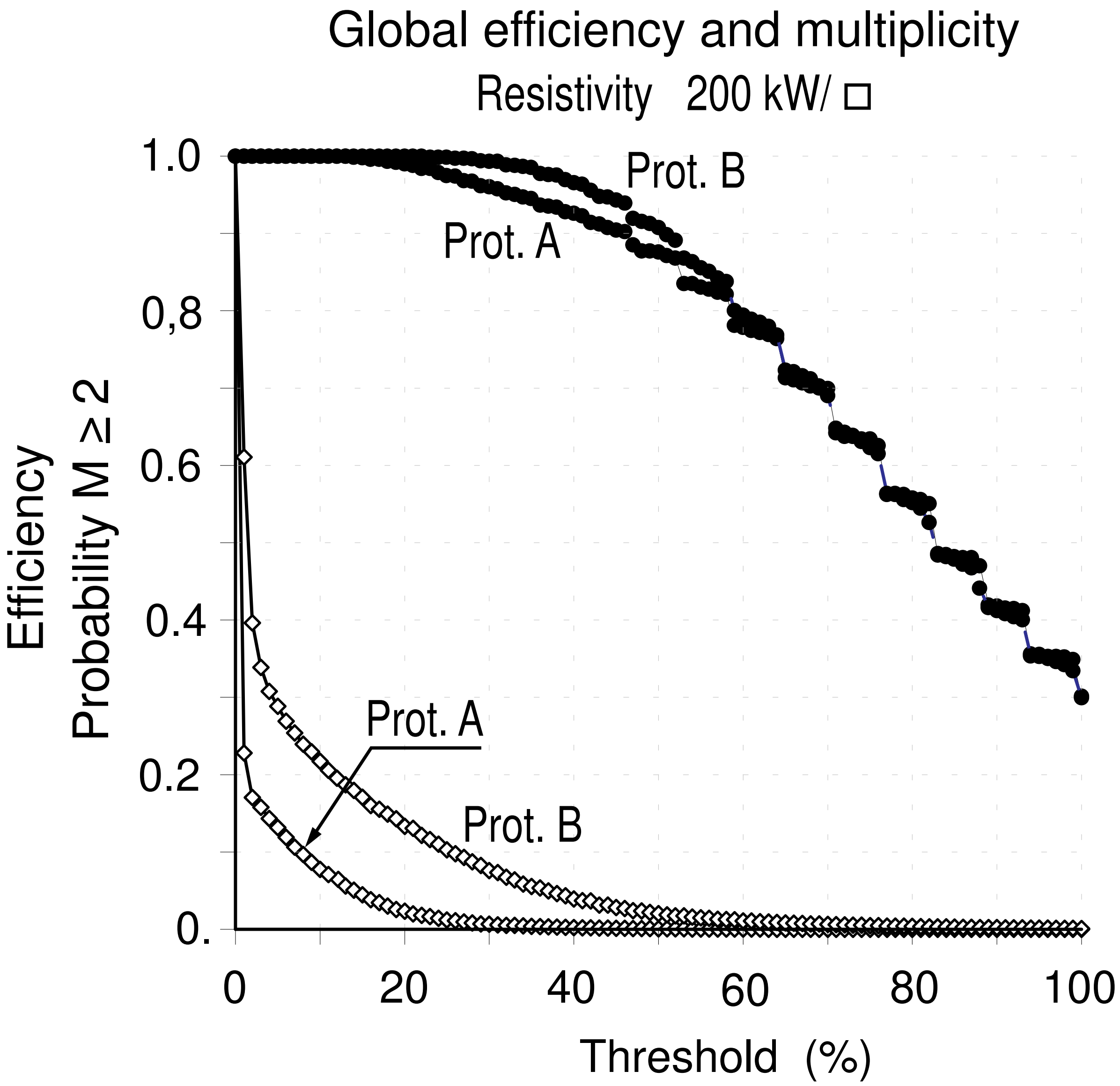


Figure 22: Simulation of a) efficiency and b) crosstalk vs. threshold for the two prototypes.

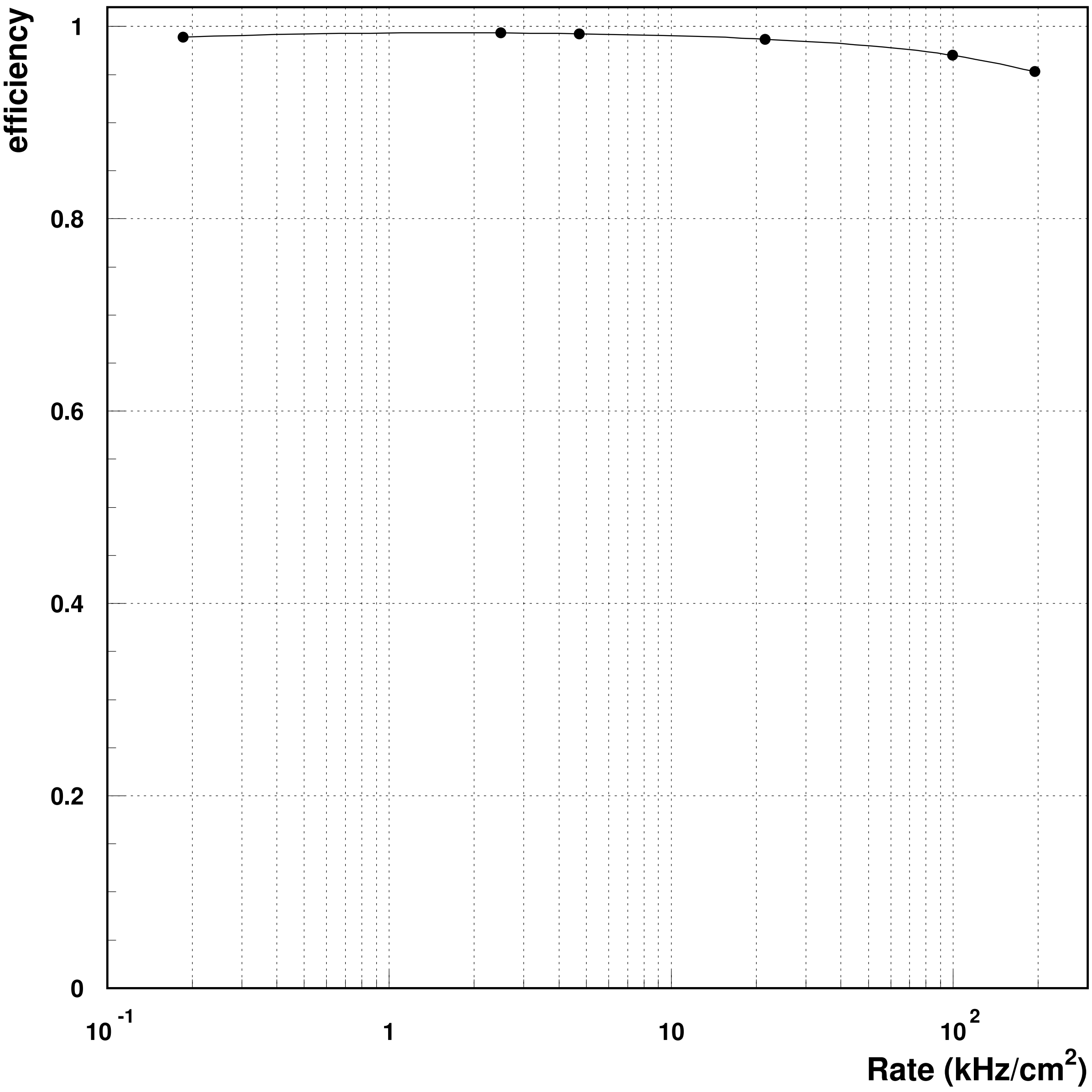


Figure 23: TGC efficiency vs. rate: prototype A

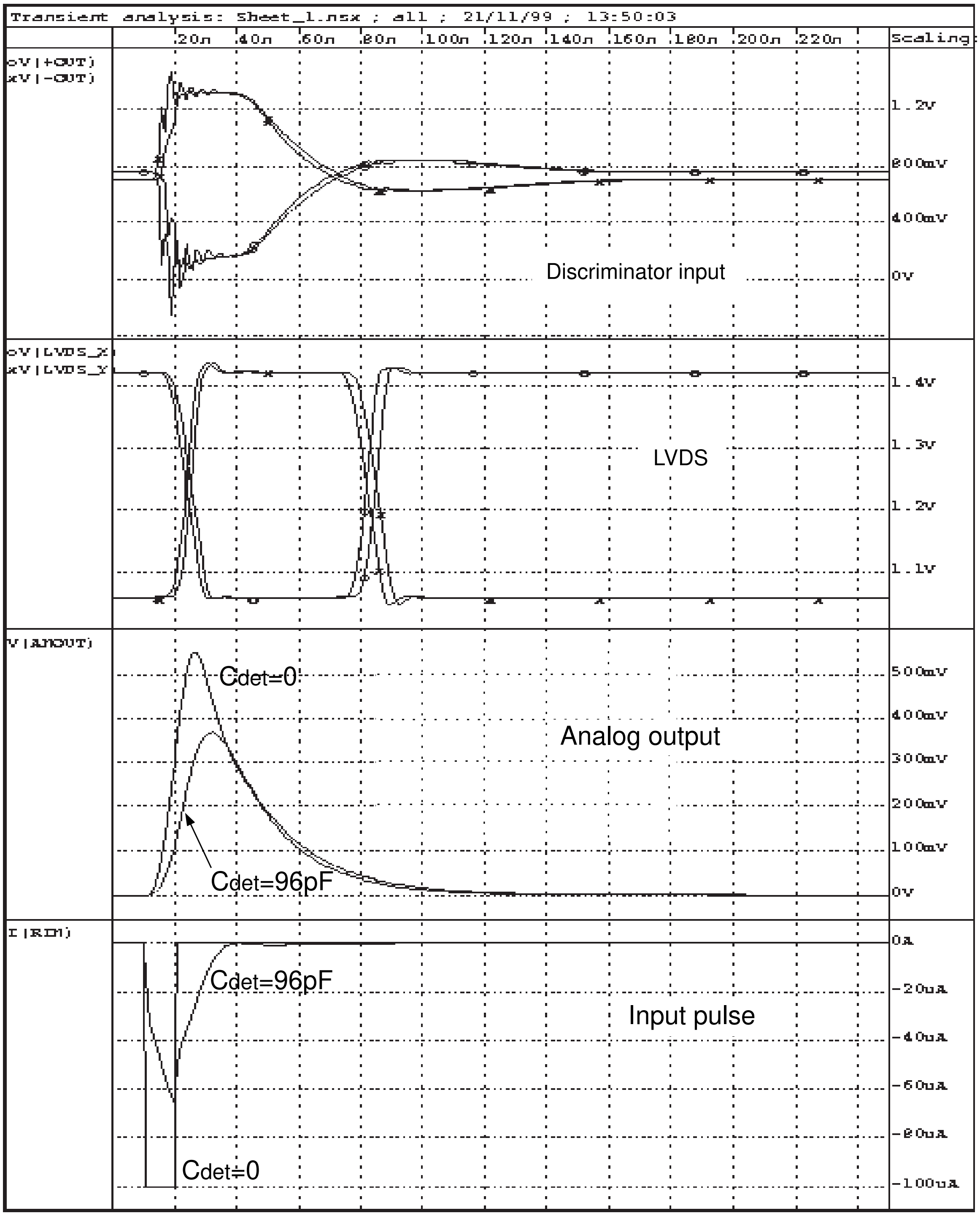


Figure 24: Simulated ASD response to short input pulse

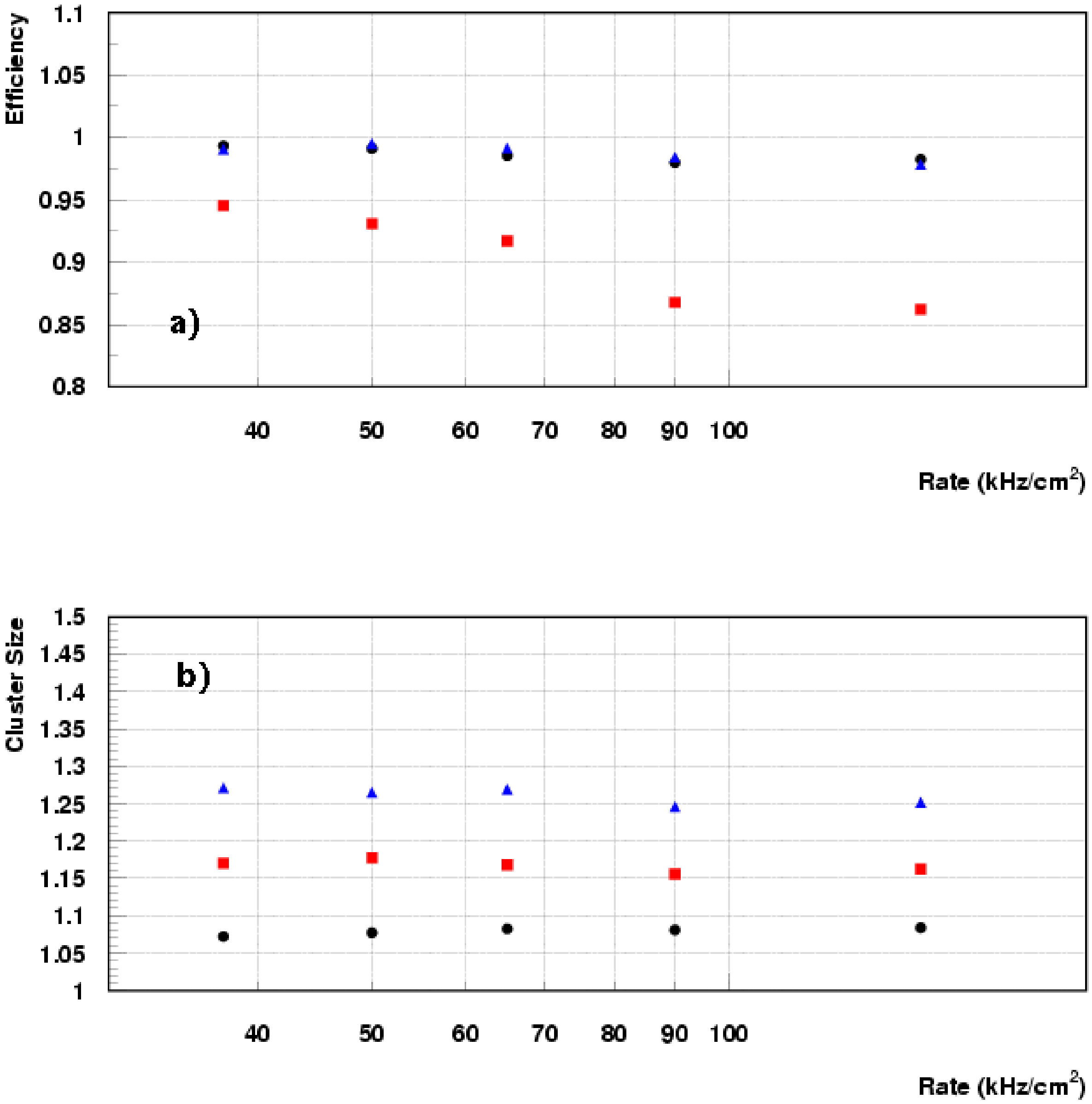


Figure 25: Prototype B: a) efficiency vs. rate, b) cluster size vs. rate

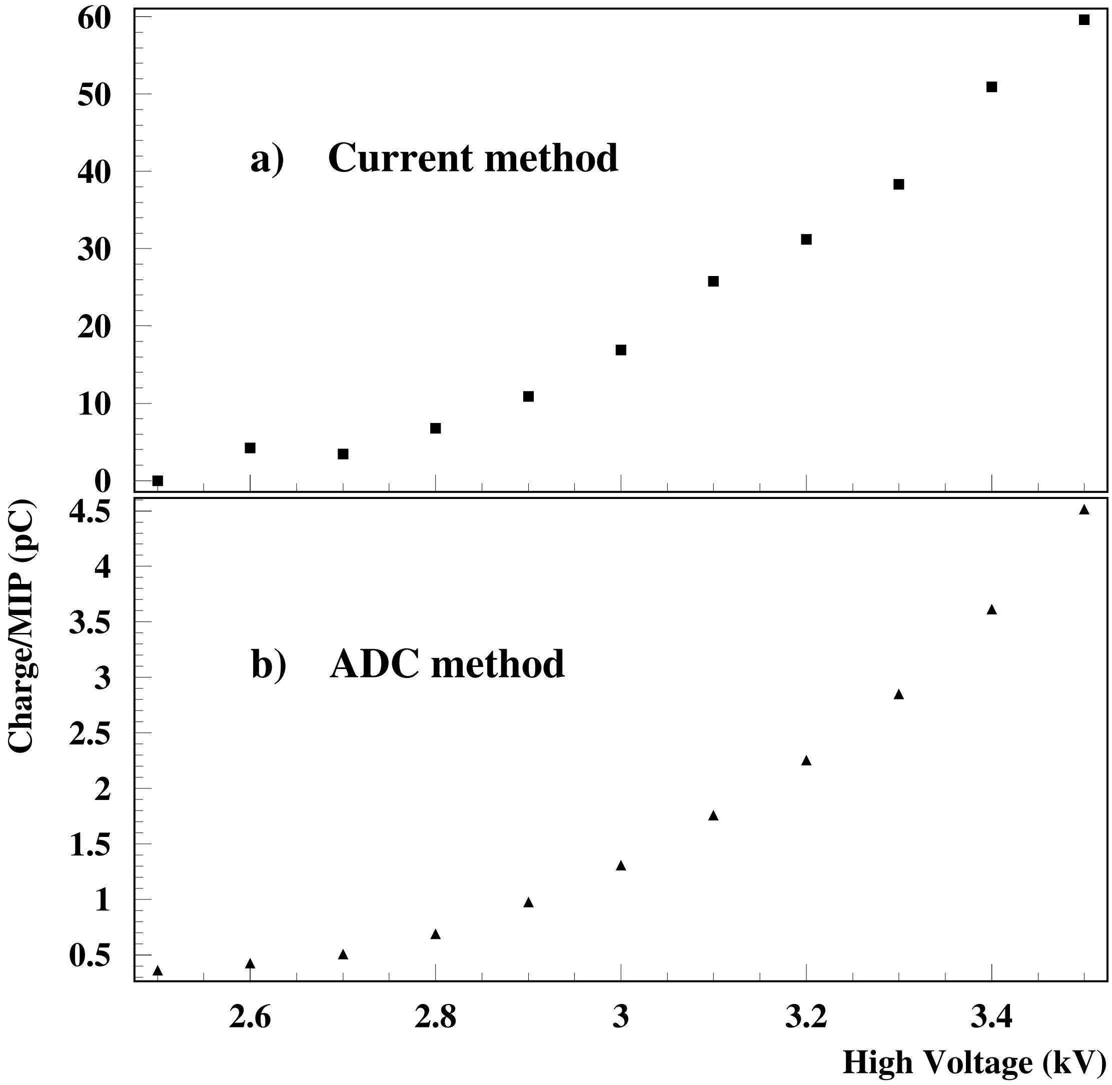


Figure 26: Gas gain evaluation: a) current method, b) ADC method.

References

[1] ATLAS muon TDR