Status of Muon TDR Preparations

Outline:

- Introduction : TDR Contents
- Software Status and New Results
- Status of Chamber Design
  - MWPC design and prototype tests
  - RPC design and related issues (-> G.Carboni)
- Status of FE-Chip and FE-Architecture
- Infrastructure and Situation with LHC cryogenics
- Planning towards TDR submission

Muon TDR Schedule

• Outline of TDR Contents	December 2000
• List of Support Documents and Authors	Mid January 2001
• **Draft of support documents**	**Begin of March 2001**
• Draft of TDR distributed to muon group	Begin of April 2001
• Technical Board meeting to discuss draft	Mid April 2001
• Final Draft: Release to LHCb	End of April 2001
• Technical Board meeting to discuss final draft	LHCb week 7-11 May 2001
• Submission to LHCC	End of May 2001
• Presentation to LHCC	4 July 2001

Muon TDR Contents

Outline:

1. Introduction (~2 p.)
   - Physics requirements
   - General Detector Layout
   - Evolution since the TP
2. Detector Specifications (~5 p.)
   - Background environment
   - Muon System Overview and Detector Technologies
     - Rate Capability, Time resolution, Cross-talk, Aging Properties
   - FE-chip requirements
3. Physics Performance (~8 p.)
   - Performance of the L0 muon trigger
   - Reconstruction of muonic final states
     - $B_d \rightarrow J/\psi K_{s,}$; $B_s \rightarrow \mu\mu$
4. Prototype Results (~15 p.)
   - Beam test results of MWPCs
   - Beam test results of RPCs
   - Test of FE-chip candidates

Muon TDR Contents

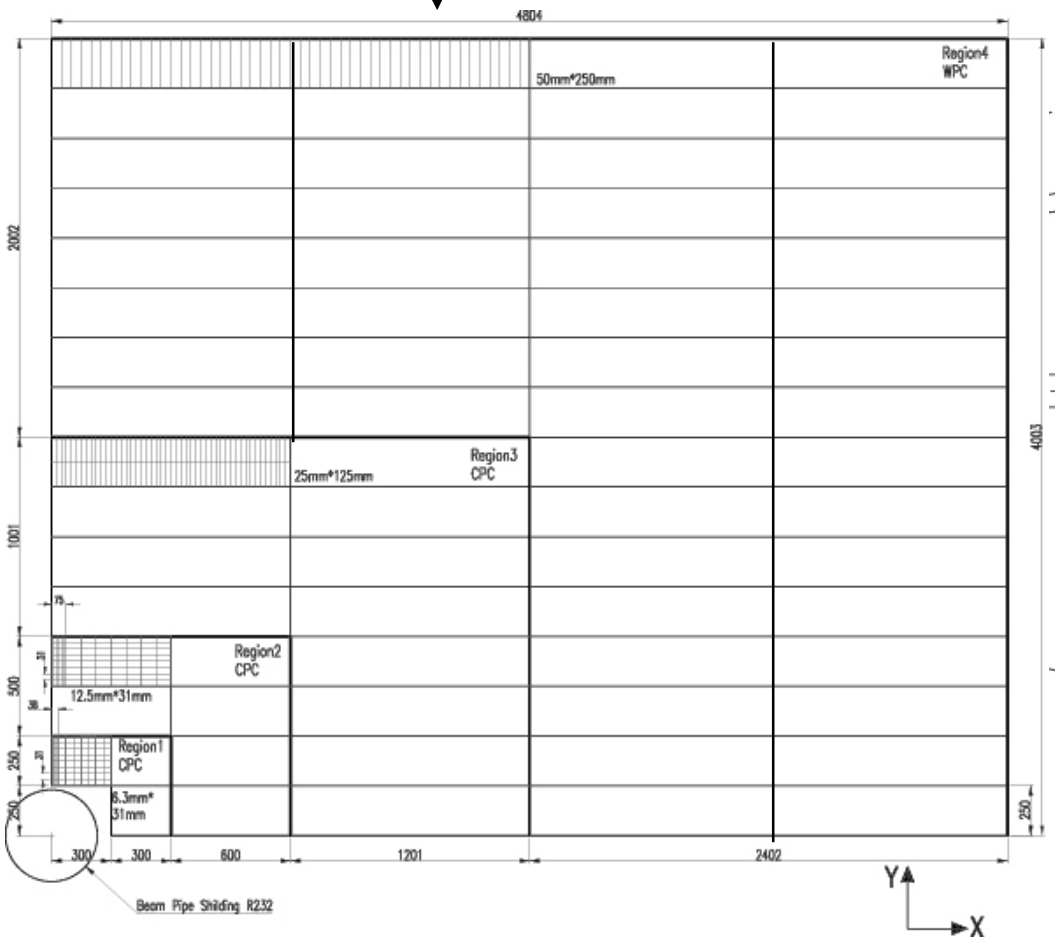
Outline (ctd.) :

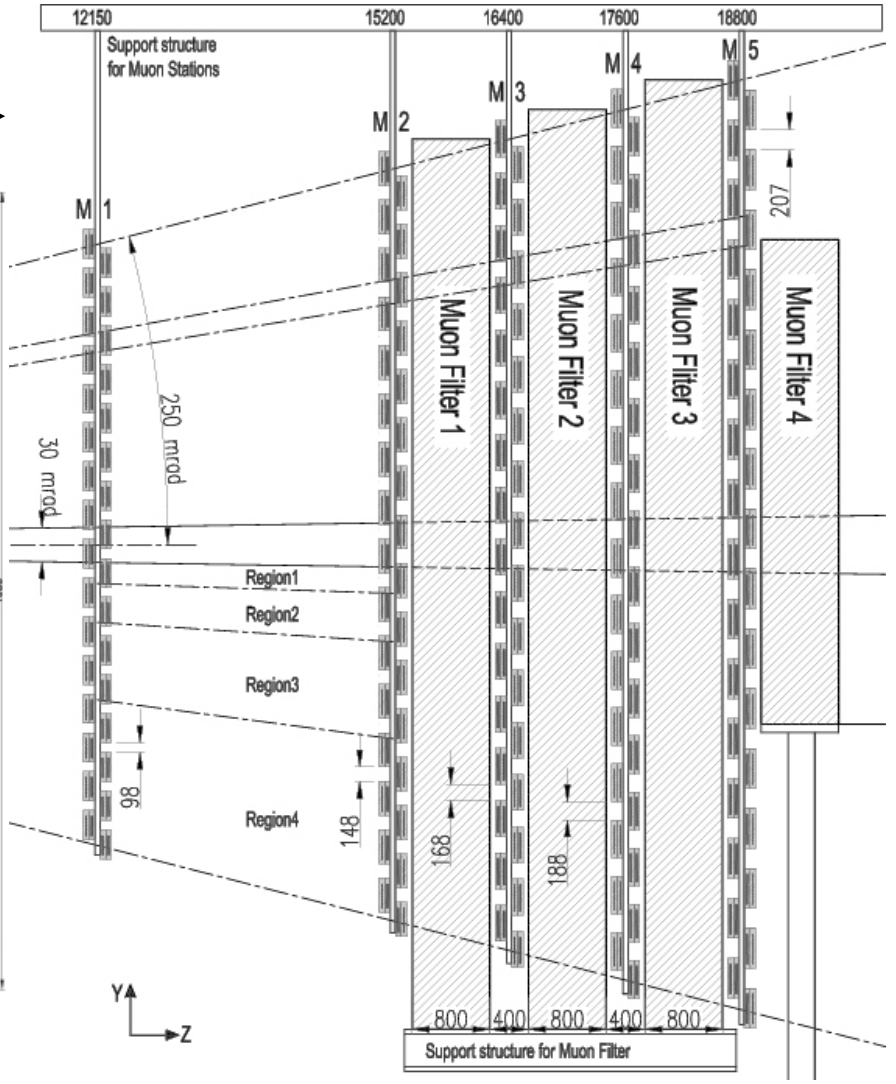
5. Technical Design (~25 p.)
   - MWPC Detector
     - Chamber design and construction
   - RPC Detector
     - Chamber design and assembling
   - Support Structures and Installation
   - Readout Electronics
     - FE-board and OR-logic
     - ODE-board, Synchronization
     - Monitoring and Controls
   - Power and Control Systems
     - Gas and HV-System
   - Safety aspects
6. Project Organization (~4 p.)
   - Schedule and Milestones
   - Distribution of responsibilities
   - Cost

Muon Detector Layout

Chamber arrangement:

Frontview ↓ Sideview →





Software Status and New Results

New Simulation:

SICBMC (incorporated in v240):

- TDR Muon Detector geometry
- Realistic chamber and material description (4- resp. 2 gap chambers)

SICBDST (incorporated in v250):

- Realistic digitization including:
- Chamber-efficiency and chamber- and electronics-noise effects
- Timing effects (time gate, time-jitter and dead-time)
- Procedure for spillover
- Cross talk
- Correct background simulation

How does the L0 Muon Trigger perform with a realisitc Muon Detector?

Software Status and New Results

Old Geometry + Old Digitization :

9795 b → μ X events, 79818 MB events (SICB v222)

MB retention		Optimal FOI [a] M_1	M_2	M_4	M_5	b → μX acc. (%) [b]	P_T (GeV/c) [b]
1%	x	3	3.5	1	1	$39.3 \pm 1.0^{+0}_{-6.7}$	$1.48 \pm 0.04^{+0.37}_{-0.03}$
	y	0.5	0.5	0.5	0.5		
2%	x	3	4.5	1.5	2.5	$53.8 \pm 0.9^{+0}_{-5.9}$	$1.20 \pm 0.03^{+0.11}_{-0}$
	y	0.5	0.5	1.5	1.5		
3%	x	4	5.5	1.5	2.5	$61.8 \pm 0.7^{+0}_{-5.6}$	$0.86 \pm 0.02^{+0.22}_{-0}$
	y	0.5	0.5	1.5	1.5		

a. Nominal background.
b. 1st uncertainty: MC statistics
. 2nd uncertainties: when maximal background is applied (i.e hits × 2 in M_1 and ×5 in M_2-M_5)

Software Status and New Results

TDR Geometry + Perfect Digitization :

36207 b→μX events, 68830 MB events (SICBMC v235). (DIGI 16)

MB retention		Optimal FOI[a] M_1	M_2	M_4	M_5	b→μX acc. (%)[b]	P_T (GeV/c)[b]	b→μX acc. diff w.r.t old simu. (%)
1%	x	2	3.5	1	1	$42.8 \pm 0.9\ ^{+0}_{-7.1}$	$1.25 \pm 0.05\ ^{+0.13}_{-0.08}$	+9±2
	y	0.5	0.5	0.5	1.5			
2%	x	2.5	4.5	1.5	2	$54.4 \pm 0.6\ ^{+0}_{-6.1}$	$1.03 \pm 0.02\ ^{+0.07}_{-0.16}$	+1±1
	y	0.5	0.5	1.5	1.5			
3%	x	3.5	5.5	2	3	$61.1 \pm 0.5\ ^{+0}_{-5.3}$	$0.79 \pm 0.02\ ^{+0.10}_{-0}$	-1±1
	y	0.5	0.5	1.5	1.5			

a. Nominal background.
b. 1st uncertainty: MC statistics
. 2nd uncertainties: when maximal background is applied (i.e hits ×2 in M_1 and ×5 in M_2-M_5

New simulation: reduced PT cut: under investigation.

Higher b→μX acc. higher at 1% MB retention. Similar b→μX acc. at 2 and 3% MB retention.

Software Status and New Results

TDR Geometry + Realistic Digitization :

37302 $b \to \mu X$ events, 59901 MB events (SICBMC v235). (DIGI 15)

MB retention		Optimal FOI [a] M_1	M_2	M_4	M_5	$b \to \mu X$ acc. (%) [b]	P_T (GeV/c) [b]	$b \to \mu X$ acc. diff w.r.t perfect digi (%)
1%	x	2.5	3.5	1	1.5	$42.0 \pm 0.9\ ^{+0}_{-5.0}$	$1.21 \pm 0.05\ ^{+0.15}_{-0.01}$	-2±2
	y	0.5	0.5	0.5	0.5			
2%	x	3	5.5	1.5	2	$53.7 \pm 0.6\ ^{+0}_{-5.4}$	$1.06 \pm 0.02\ ^{+0.06}_{-0}$	-1±1
	y	0.5	0.5	1.5	1.5			
3%	x	4	5.5	2	3	$60.7 \pm 0.6\ ^{+0}_{-5.0}$	$0.80 \pm 0.02\ ^{+0.12}_{-0}$	-1±1
	y	0.5	0.5	1.5	1.5			

a. Nominal background.
b. 1st uncertainty: MC statistics
. 2nd uncertainties: when maximal background is applied (i.e hits $\times 2$ in M_1 and $\times 5$ in M_2-M_5

Performance similar to perfect digitization

Software Status and New Results

Parameters used:

- Chamber efficiency: 95%
- Chamber noise: 100 Hz/cm2 for RPC
- Electronics noise: 100 Hz/channel
- Time gate: 20ns
- Dead time: 60±10ns
- Cross talk: included for R3+R4
- Spill-over: 0.36 interactions/bunch crossing

Conclusion:

- Trigger results obtained with old and new simulation are similar.
- The P_T cut decreases up to 0.3 GeV/c. This is under investigation.
- "Perfect" and "Realistic" digitization give similar results.

New Muon System Notes

- **LHCb 2000-016, , 22 Dec 2000, P. Colrain et al.,**
  Optimization of muon system logical layout
- **LHCb 2001-002, 30 Jan 2001, S. Amato et al.,**
  Simulation of detector response of the LHCb Muon System . . .
- **LHCb 2001-007, January 2001, G. Martellotti et al.,**
  Monte Carlo samples and efficiencies for the muon system optimization
- **LHCb 2001-009, Feb 2001, E. Polycarpo et al.,**
  Muon Identification in LHCb

MWPC Design and Construction Status

Design Specifications:

30μm wire, 1.5mm wire spacing, 5mm gap size, 2x2gaps

->All chamber parameters defined since July 2000

Chamber Components:

- Panels
- Cathode PCB layout
- Wire-fixation-bars (Frames)
- Gap-bars and Gas-Connections
- HV- and FE-Interfaces

-> Baselines defined, some parts need more tests

Design and Construction Issues:

- single vs. double gap construction
- wire soldering

->Keep choice between options open still

Chamber Components

Panels:

-> Key element in MWPC,

± 50μm precision over 40cm x 140cm required

Candidates:

1. **Honeycomb:** Light, robust, good gluing properties, precision panels are expensive

2. **Chempir Core:** Can be produced with good planarity at a reasonable price, gluing problems have to be solved

3. **Polyurethanic foam:** very robust and very fast to produce, good planarity of large surfaces to be proven (promising) density 0.5 g/cm^3 (X_0 in M1 should be <10%) ε_r ~ 2-3 no problem, cost very promising

-> 6-7 mm Honeycomb Panels baseline at present

Chamber Components

Frames:

1. **Wire-Fixation-Bars (long edge):**

   Solution which does not require precision on wire-fixation-bars has advantages (cheaper, easier to build)

   -> Precision could come from special spacers/jigs introduced every 10-15cm in the wire-fixation bars

   Wire fixation bars can also be used to group signals to required pitch for subsequent connector.

2. **Gap-Bars (short edge):**

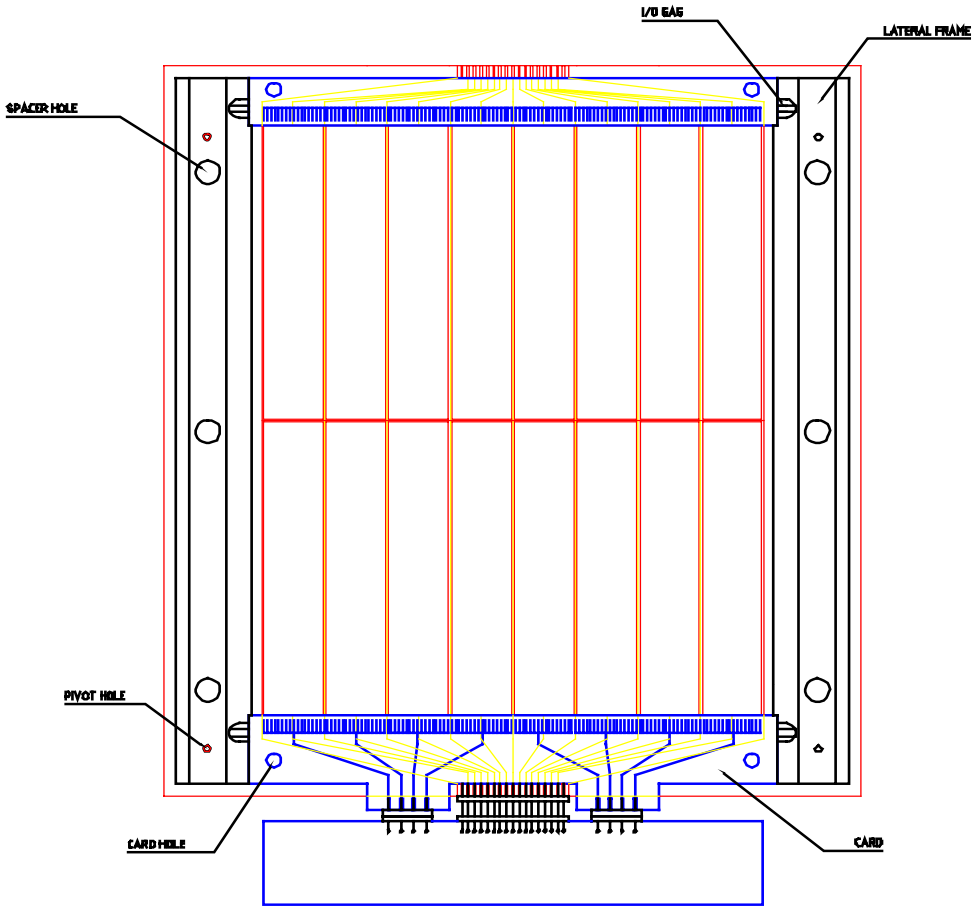
   Could be of one piece precisely 5mm thick.

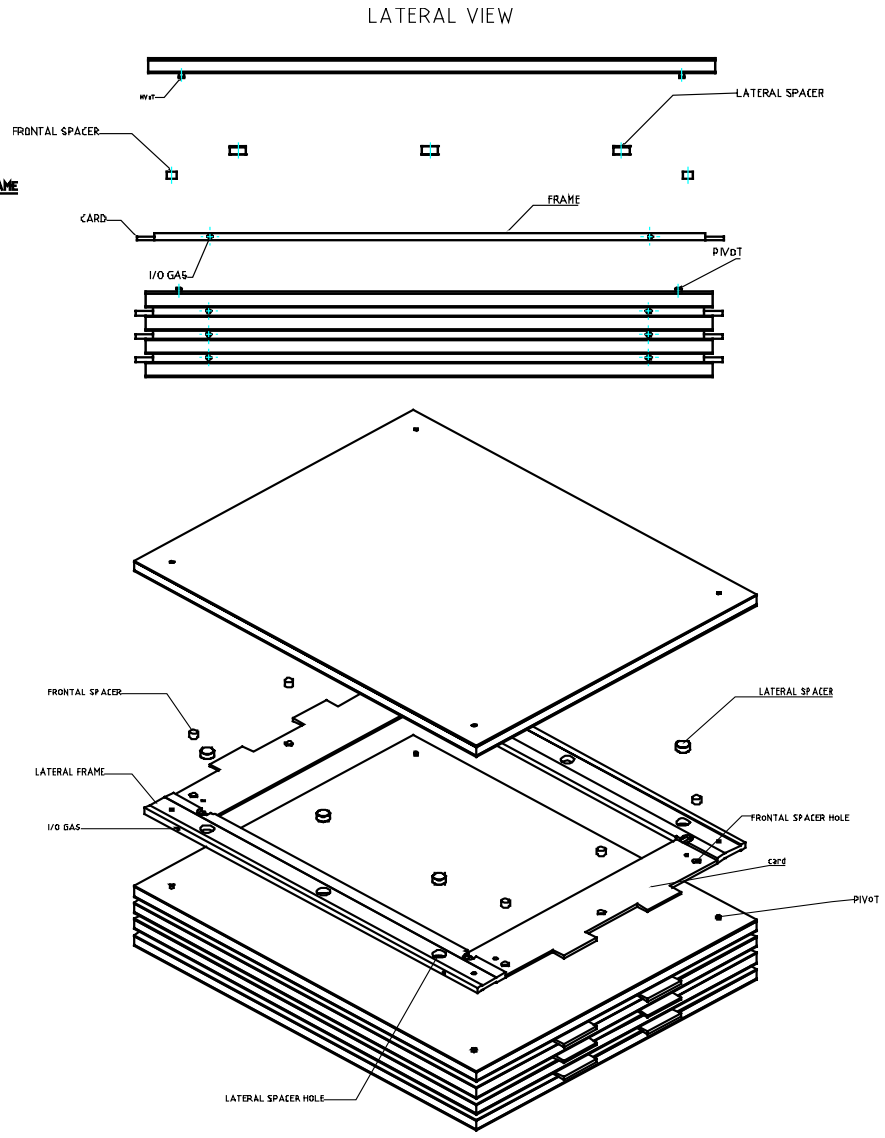
   Possible materials: Aluminum, Stesalite

   -> Use them to bring the Gas in

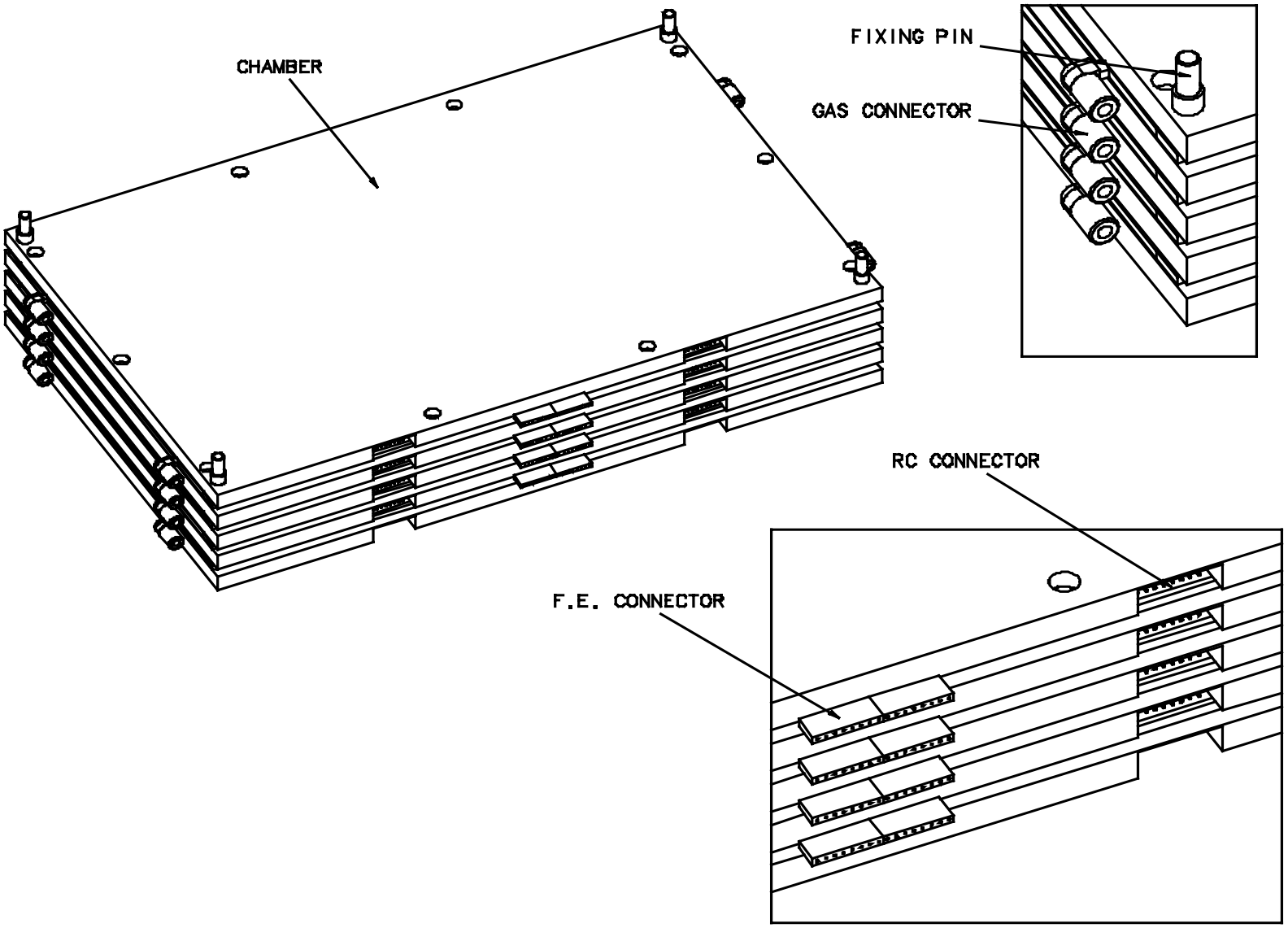
   -> 2 independent gas cycles foreseen in the chambers to enhance redundancy;

Chamber Design





Chamber Design



Chamber Components

HV- and FE-Interface:

1. **HV-Distribution, Resistors and Capacitors:**

   Capacitors are a delicate element in the chambers.

   Foresee easy replacement and tests independent of chambers

   -> Mounting on a separate board seems preferable

3. **FE-Interface:**

   Try to minimize number of different types of FE-boards.

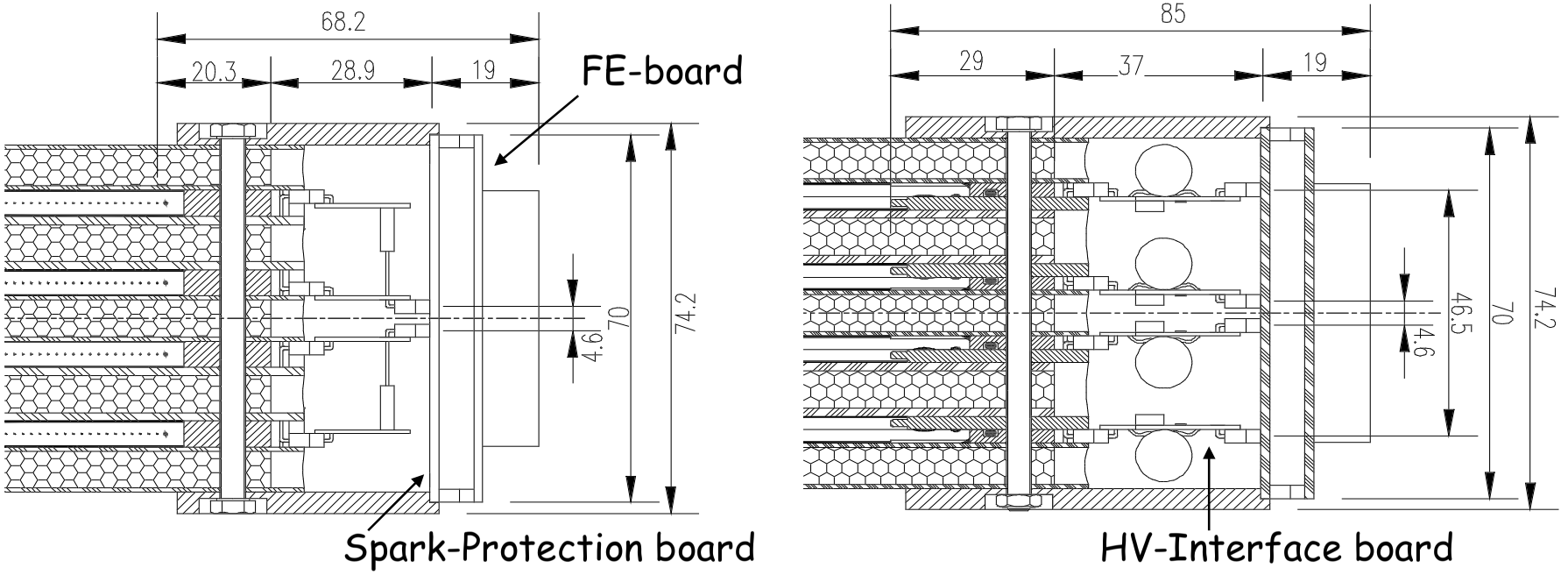
   Different requirements for various regions (Anode/Cathode readout, granularity variations, different technologies etc.)

   -> Agreed on single FE-board per technology and polarity, usable in all regions, with 16 FE-channels

-> Distance between sensitive area and border of chamber (including electronics) should be kept small (sum of both sides < 10-12cm)

Chamber Border Region

Possible Cathode- and Anode-readout:



Space Requirements:

Top with Anode/Cathode Readout:	85mm
Bottom with Cathode readout	70mm
Bottom no readout	35mm
Side no readout	50mm
Side with Cathode readout	60mm

Chamber Construction

Wiring (Gap construction):

Double gap

- more tests required to prove precision for long panels
+ wiring machine simple, allows work in parallel (wiring, gluing)
- 2 planes per wiring
+ symmetric load on panel

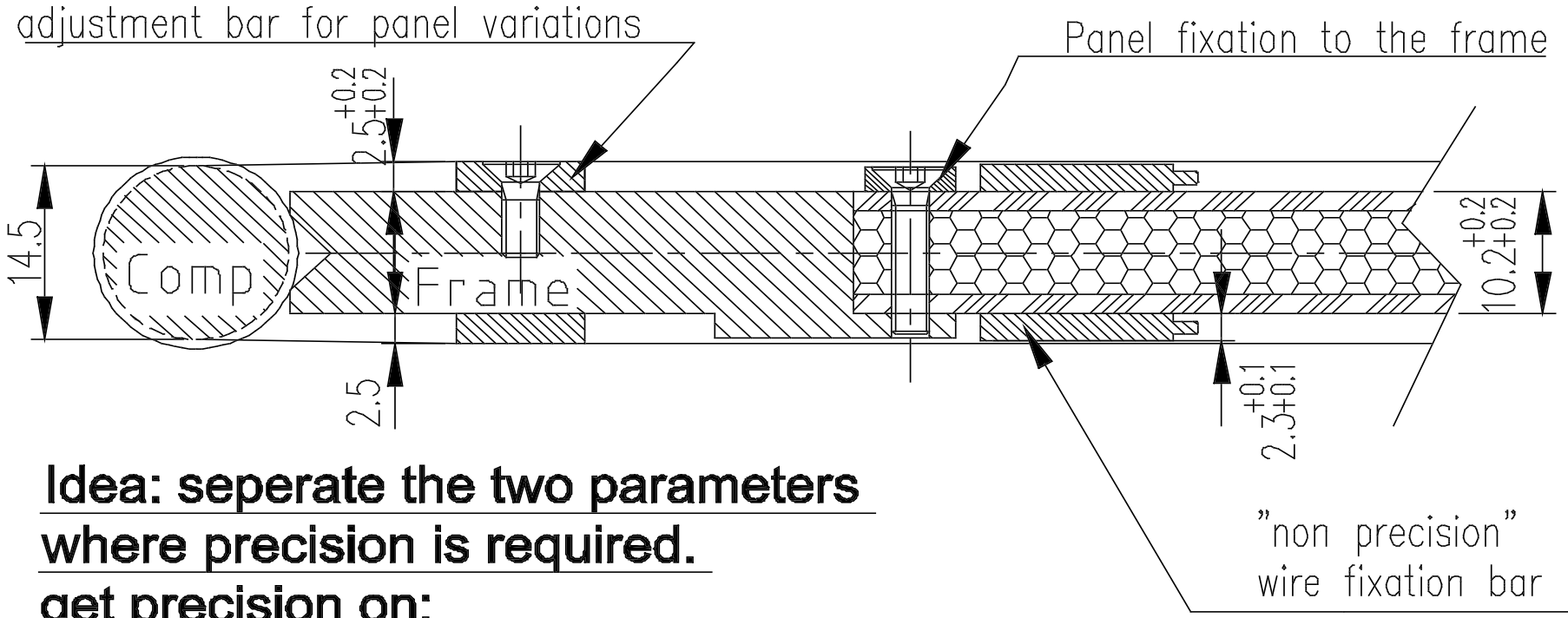
. . .

Single (Multi) Gap

+ required precision can be kept even for long panels (150cm)
- wiring machine complex, requires special fast gluing procedure
+ 8 planes per wiring
- asymmetric load on panel

. . .

Double Gap Wiring: Principle

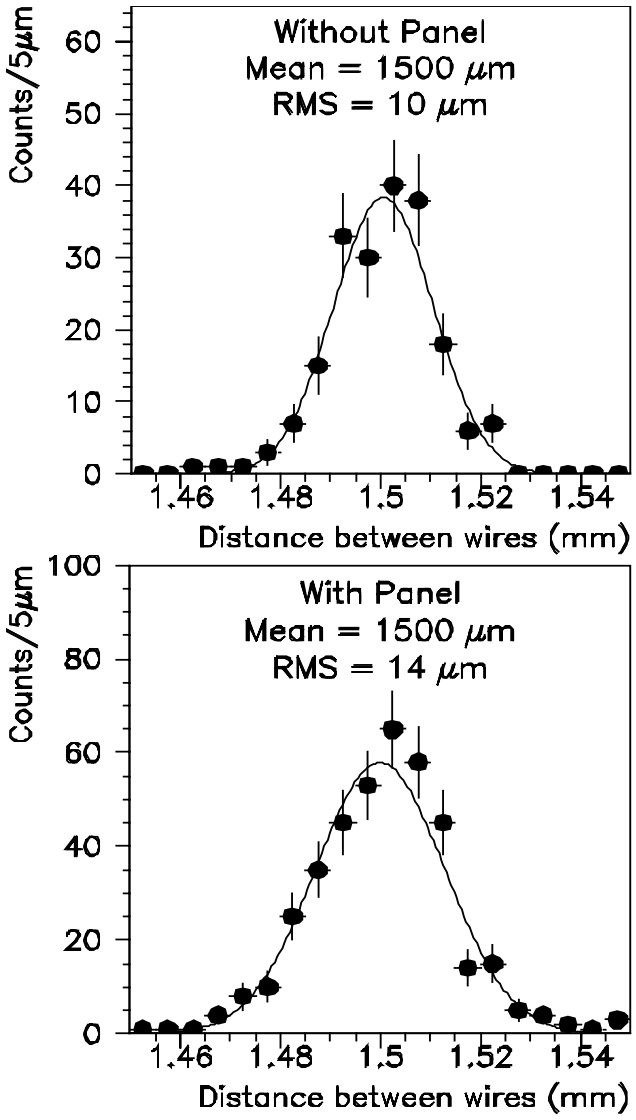


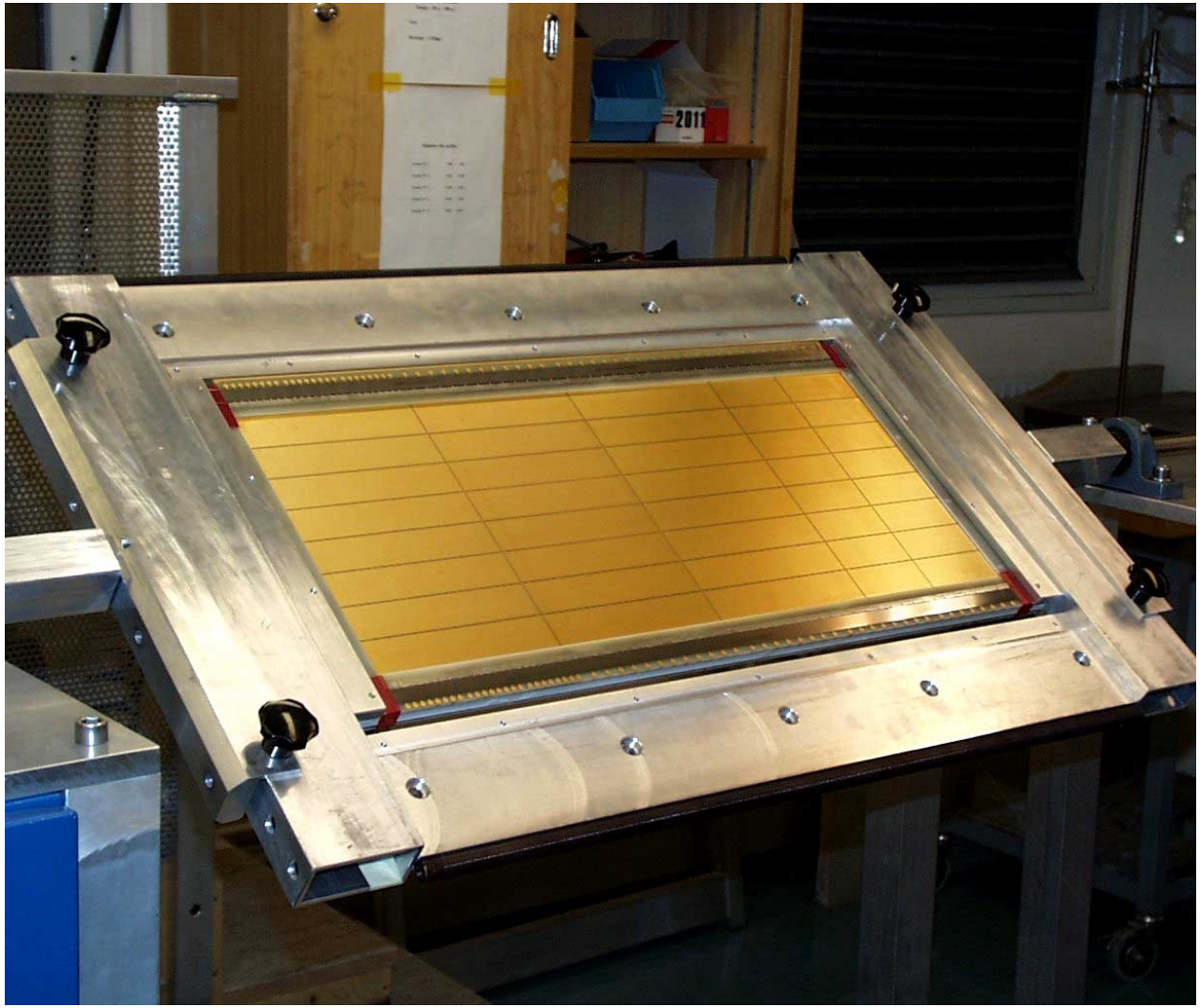
Idea: seperate the two parameters where precision is required. get precision on:

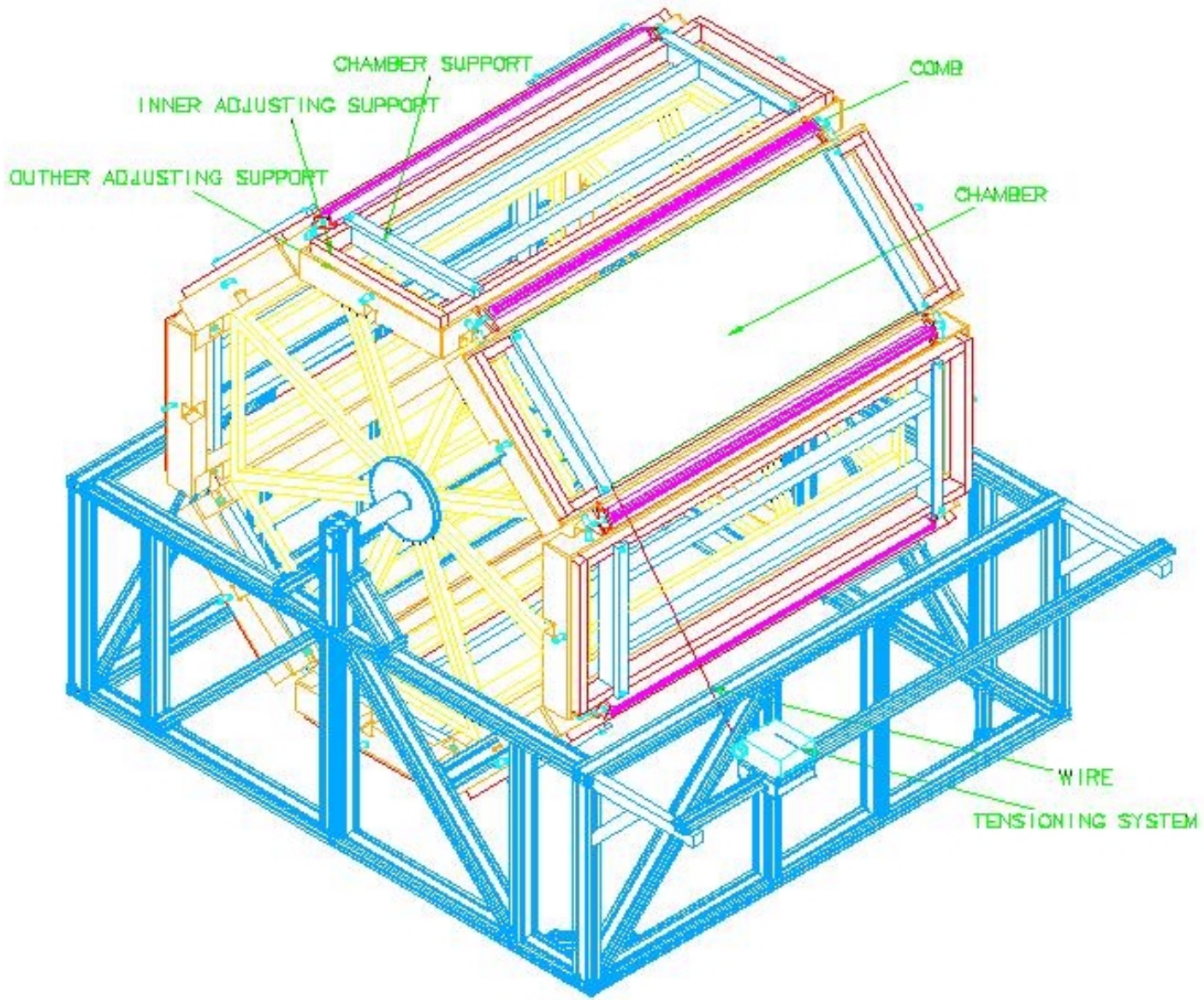
1) wire spacing (1.5mm) from the comp
2) Anode-cathode distance (2.5mm) from the adjustment bars

-> Up to 700mm panel length no problem with precision

Double Gap Wiring: Results





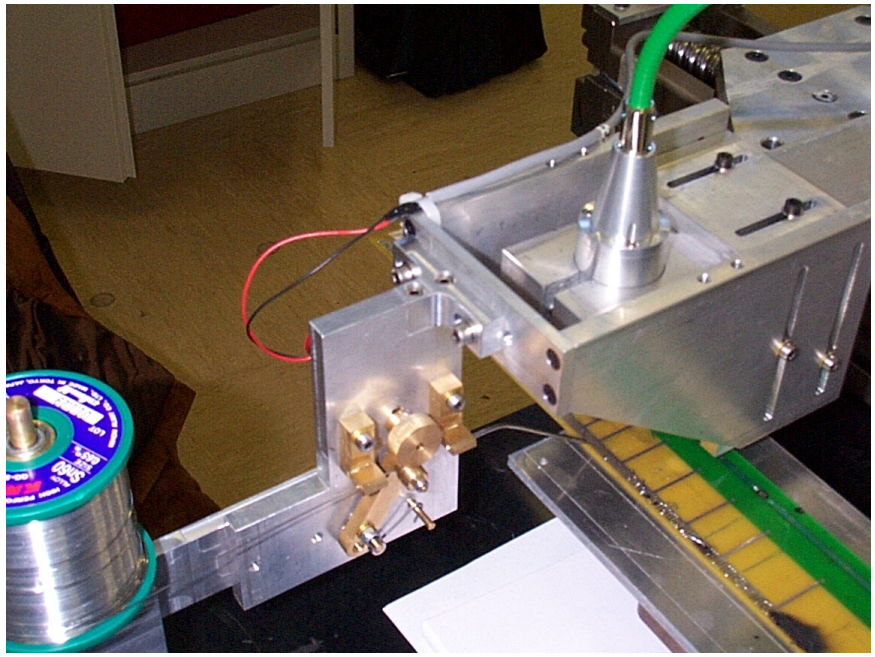

CHAMBER SUPPORT
COMB
INNER ADJUSTING SUPPORT
OUTHER ADJUSTING SUPPORT
CHAMBER
WIRE
TENSIONING SYSTEM

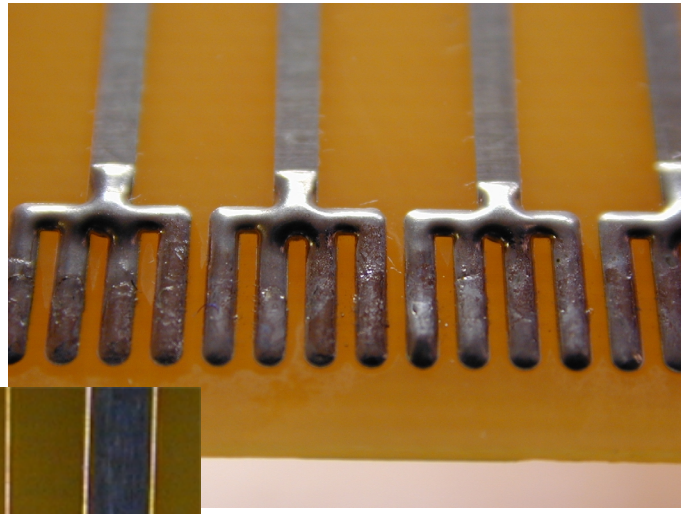
Chamber Construction: Wire Soldering

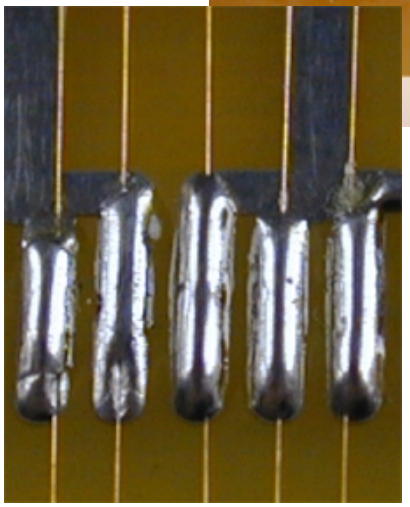
Number of wire soldering points: 4.86×10^6 !

-> Most time consuming task in chamber construction (1.5mm wire spacing)

-> Automated Wiring procedure mandatory for MWPC construction







- First promising results at LNF with soldering using a laser beam
- Try to use low T soldering paste

Conclusion and Plans

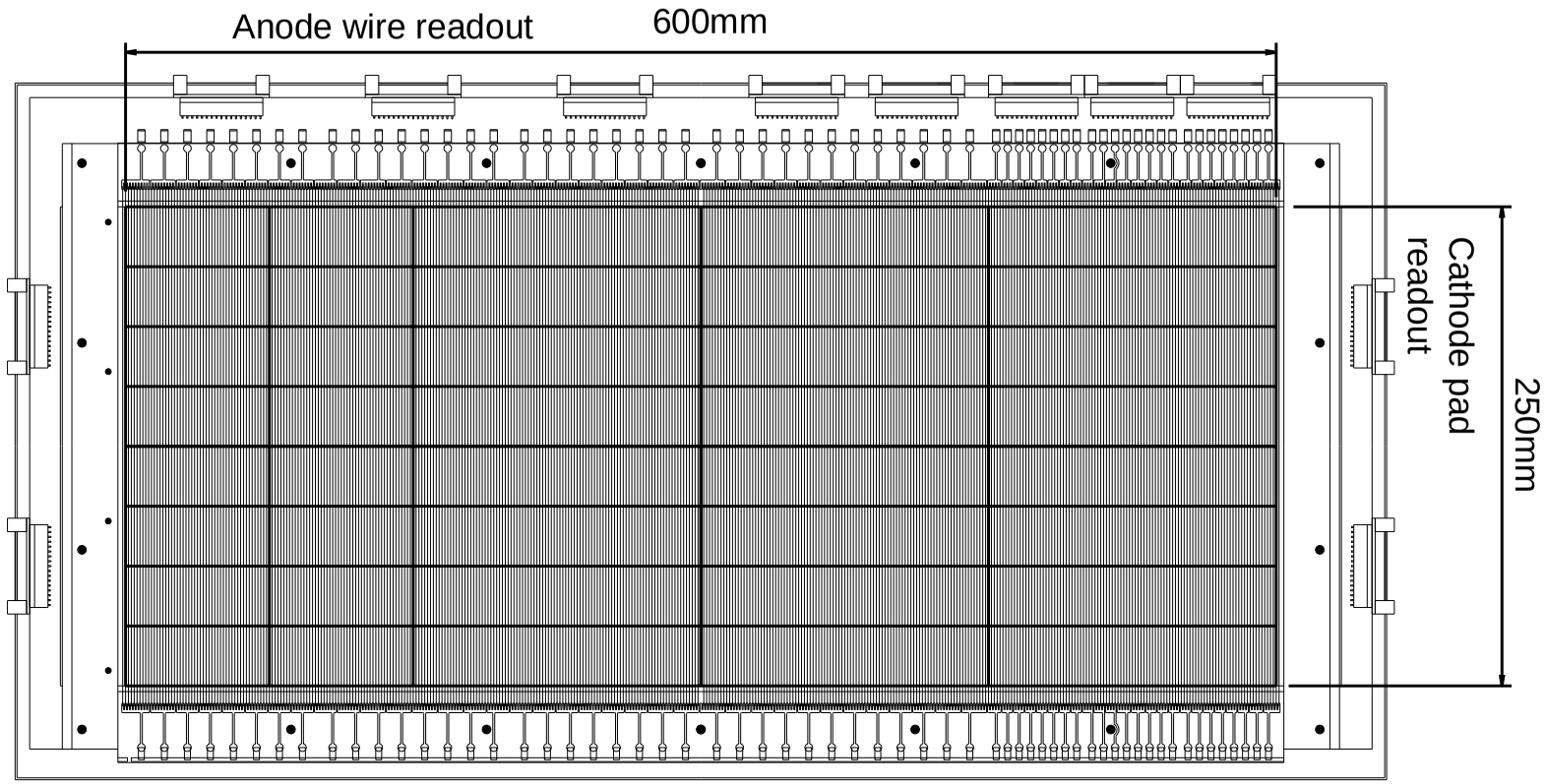
- Good progress has been made towards a chamber design which is robust and simple.
- All chamber components have been defined
  -> Baseline chamber design ready
- Ideas are evolving on chamber construction
  -> Keep various options open
- Notes on design and construction are under preparation:
  - LHCb 2001-026, **March 2001, CERN, Ferrara,LNF, PNPI, Rio**
    Design and Construction of MWPC detector for the LHCb Muon System
    -> Draft to be ready by March 20

Other related notes:

- LHCb 2001-008, **15 Feb 2001, G. Auriemma et al.,**
  Test results of Chempir Core Panels for the MWPC
- LHCb 2001-032, **March 2001, LNF and CERN,**
  Support Structures for Muon Chamber and Iron filter

MWPC Prototype Test

Full scale 4-gap prototype for M2R2:



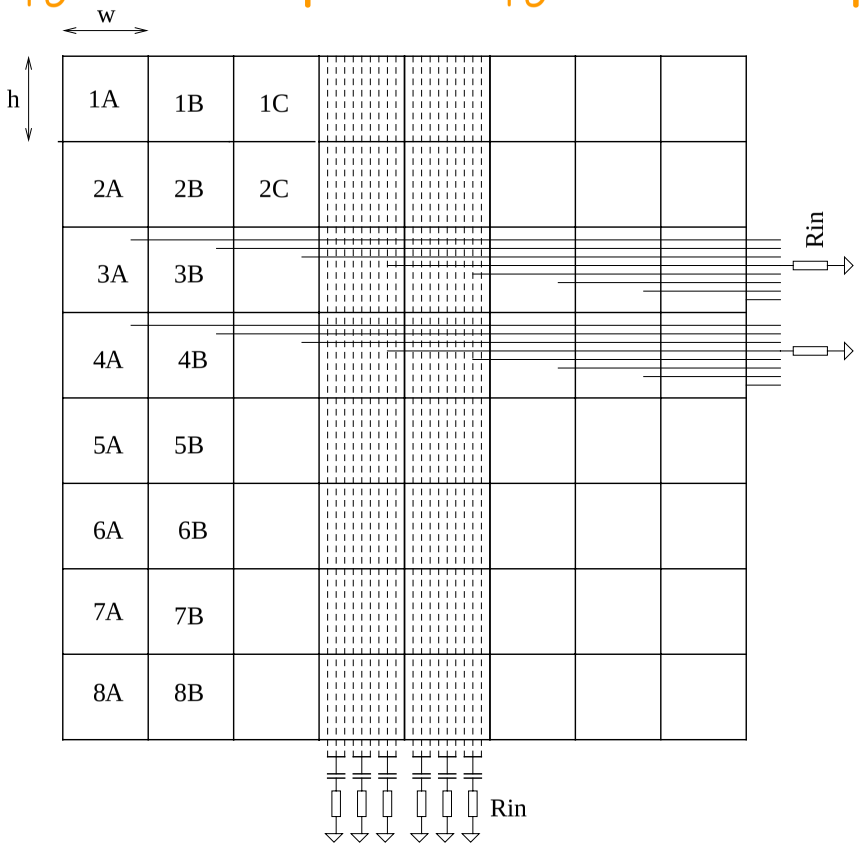
- LHCb 2001-024, **Feb 2001, D. Hutchcroft et al.,**
  Results from the MWPC prototype for the inner part of the LHCb Muon System
- LHCb 2001-025, **Feb 2001, B. Bochin et al.,**
  MWPC test results with latest PNPI prototype and SONY chip etc.

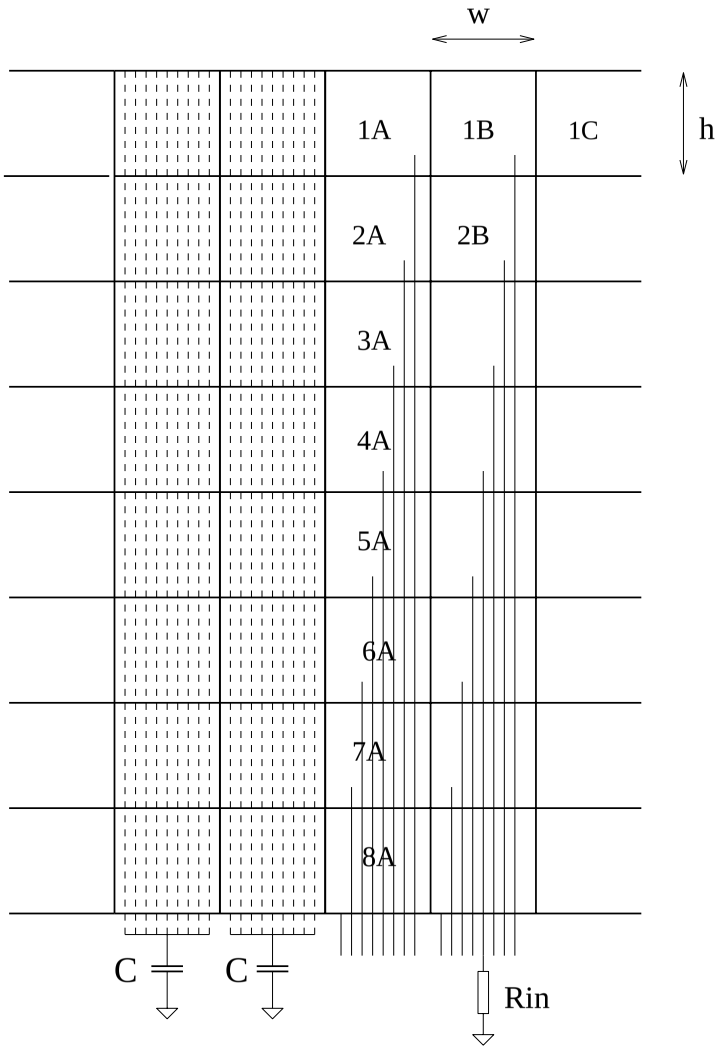
Chamber Components

Cathode PCB layout:

M2-M3(5) R1 M2-M5 R2 ⟶

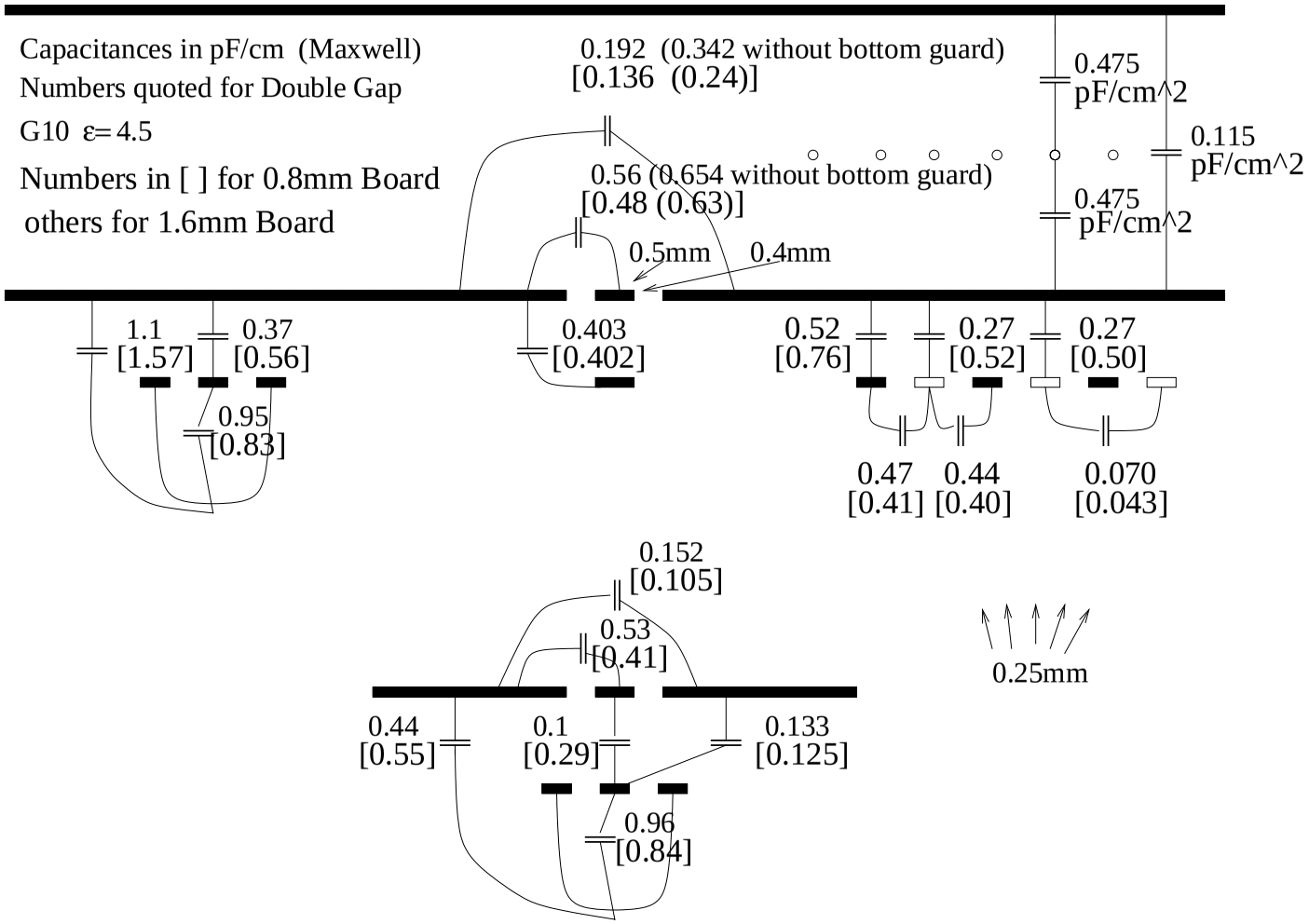
C_{PG} ~ 30-55 pF C_{PG} ~ 45-120 ? pF





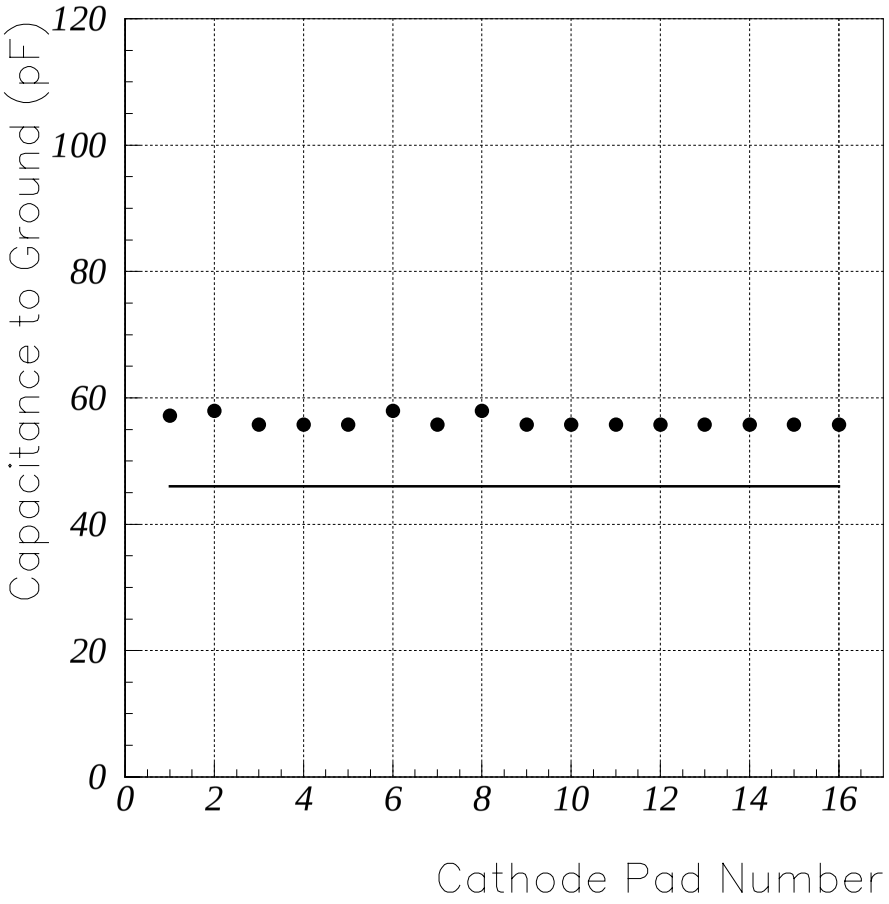
Chamber Components

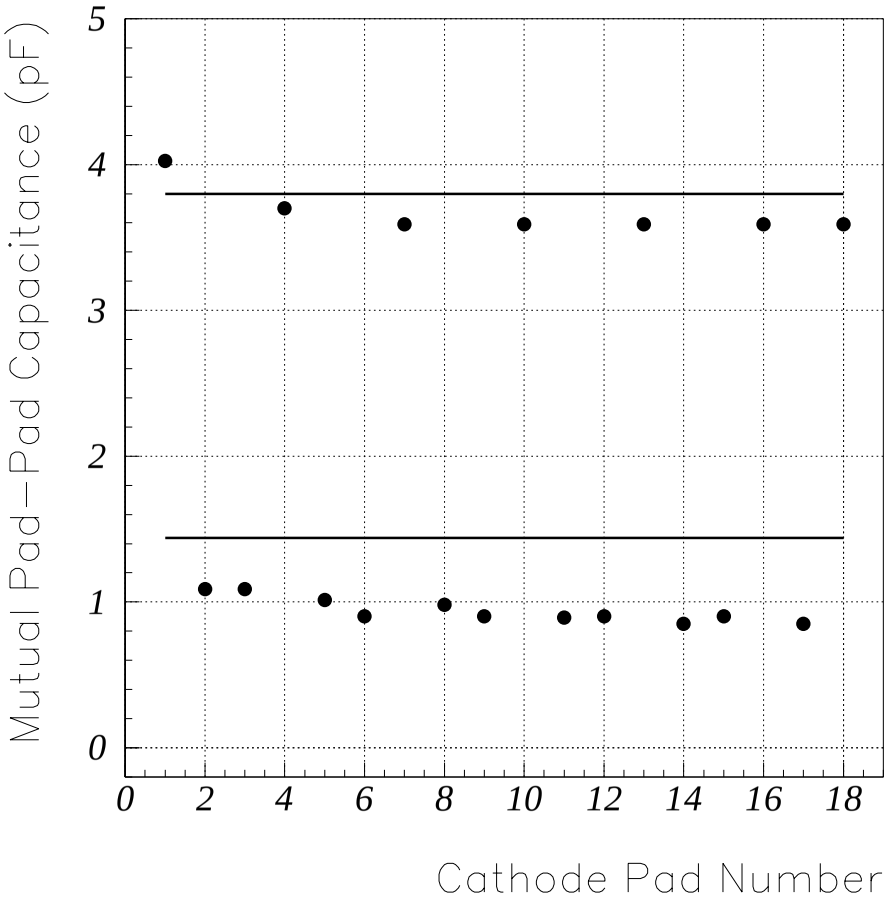
Readout Traces: 3-4 layer PCB doesn't help, but is ~twice more expensive !



Cathode PCB

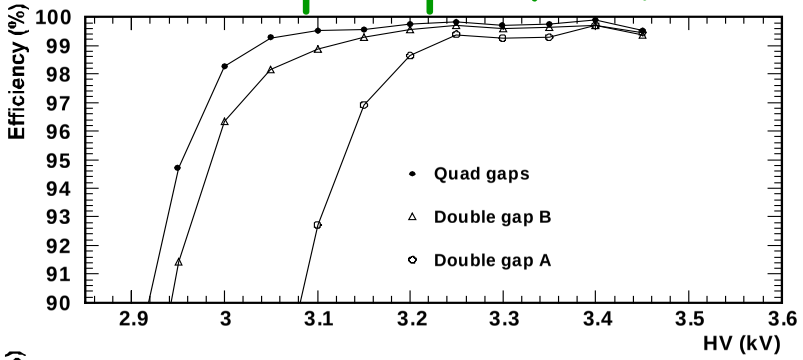
Comparison Simulation - Measurement for Capacitance:

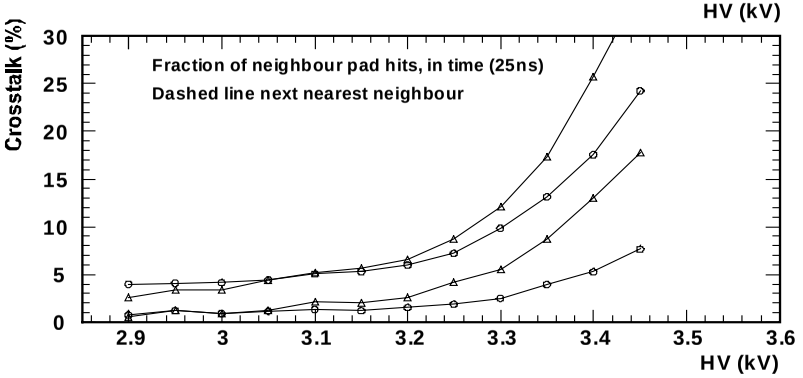


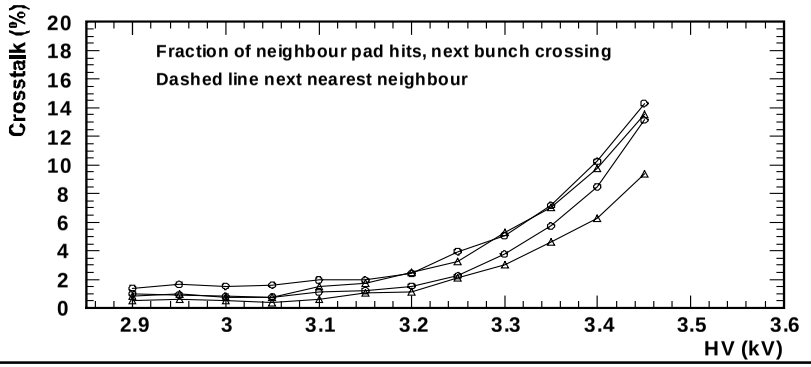


Prototype Tests Results

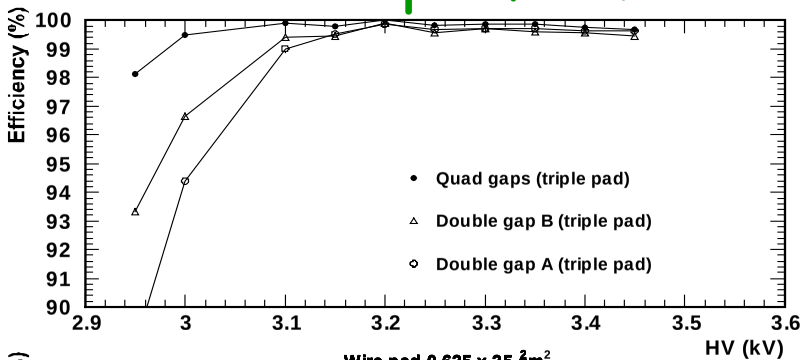
Cathode pad performance:

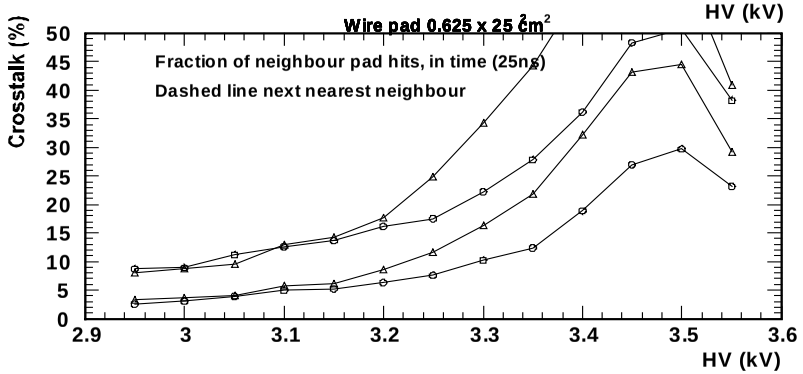


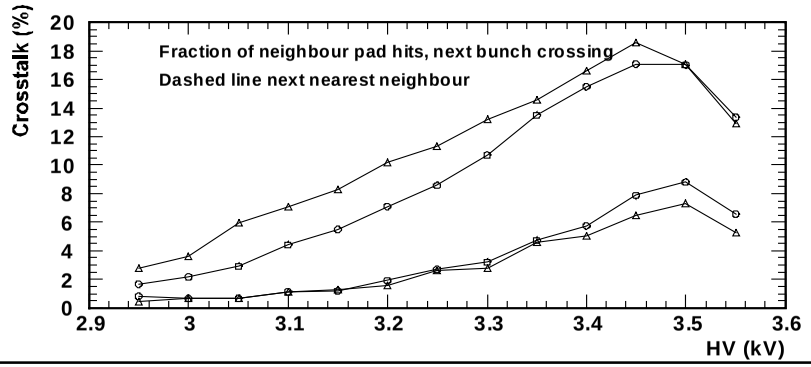




Anode wire performance:

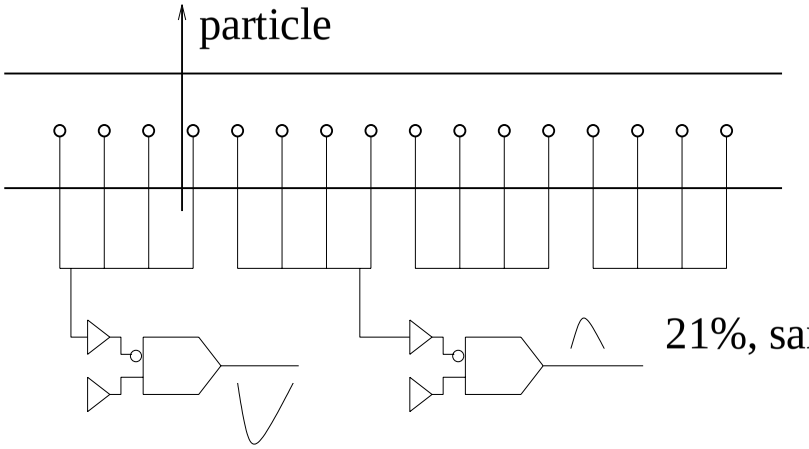


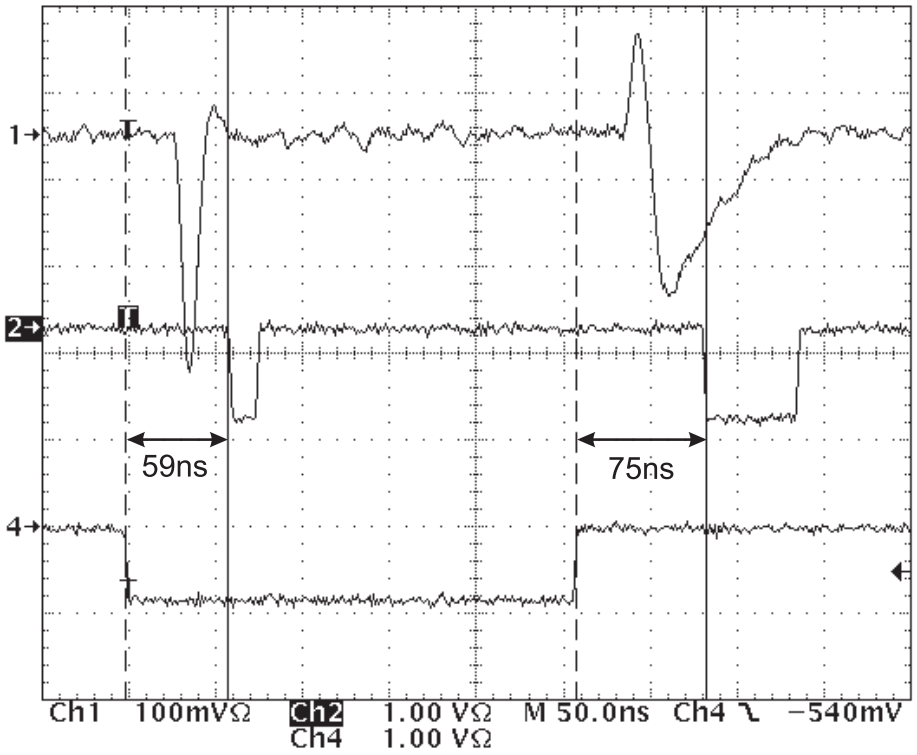




Prototype Tests Results

Origin of "late cross-talk" on wire strips:





"Late cross-talk" at the level of few % might be acceptable.
Further studies needed

ASDQ Chips

ASDQ: (M.Newcomer)

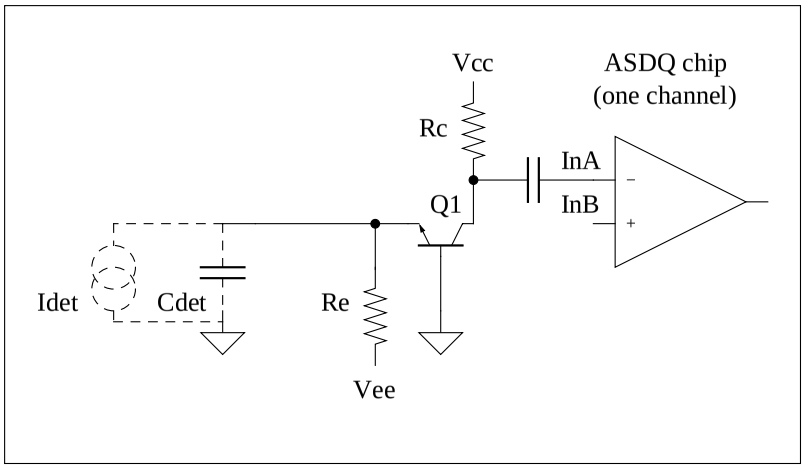
ASDQ chip well adopted for our application, except for

- R_{in}=280 Ω -> limited range of C_{det} (< 50 pF)
  -> Cross-talk
- non symmetric BLR: -> needs further investigation

ASDQ++: (A.Kachtchouk)

Add Common Base Transistor:

- > R_{in}= 25 Ω



ASDQ':

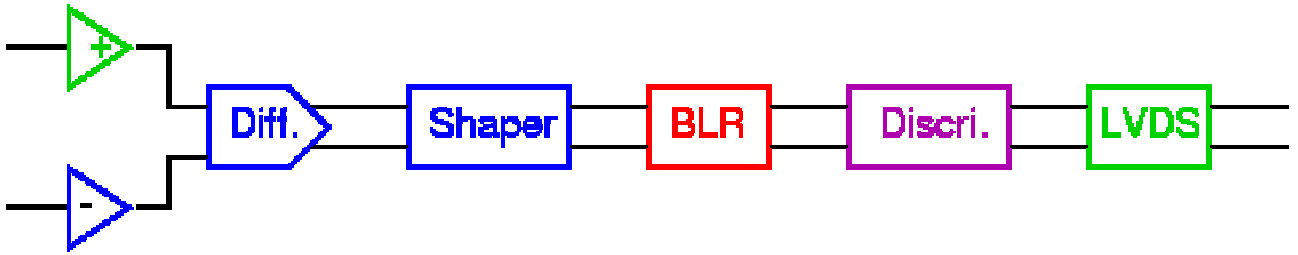
- ASDQ can be produced with R_{in}= 50 Ω
- BLR could be modified

-> Cost: ~ 120 kCHF Time: 1 year until chips could be delivered

CARIOCA

CERN And RIO Current Amplifier

(D.Moraes, F. dos Santos, P.Jarron, . . .)



- Design and Test of Preamplifier (pos. polarity) Jan 2000 -Feb 2001
- Design/Layout of Shaper and neg. polarity input submis. 28 Feb 2001
- Design/Layout of Discriminator submis. 30 Apr 2001
- Design/Layout of BLR and Test of Shaper/pos. pol. submis. 30 Aug 2001

-> Important Milestone for the CARIOCA Project

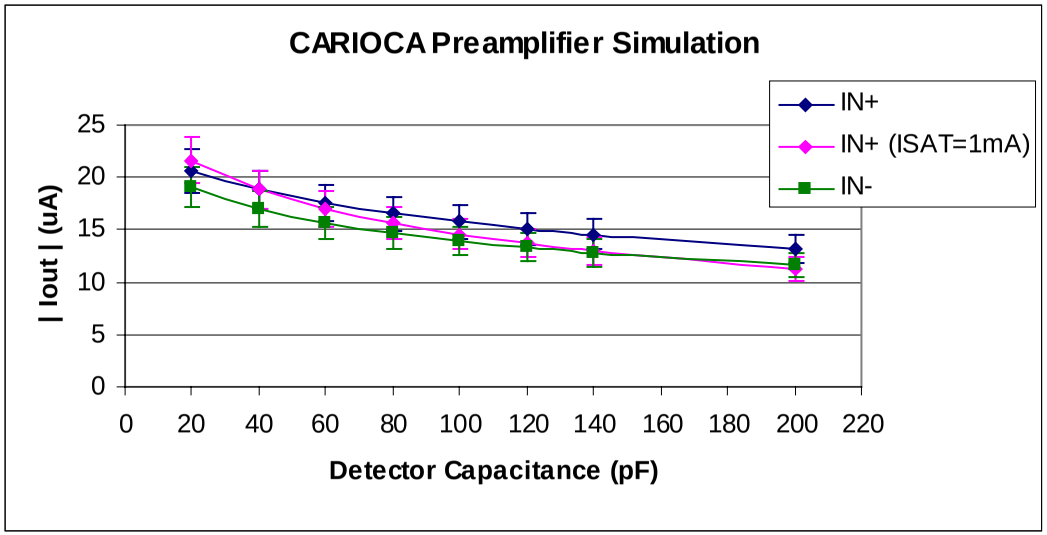
- Test of full chip and final corrections submis. Feb. 2002
- Engineering Run summer 2002
- Final Chip available end 2002

CARIOCA Results: Summary

- **CARIOCA** has a peaking time of 14ns @ 0pF . We expect a t_{peak} of 7ns only from the preamplifier.
- The circuit is stable for a detector capacitance up to 120pF; this can be further improved in the next versions.
- Noise measurement indicates an excellent performance of the current mode feedback.
- Time walk of 5ns for a Q_{IN} up to 150fC and a negligible t_{walk} for higher charges.
- Up to now the CARIOCA showed a good channel uniformity (within 10%), but there are still test to be done with the 14-ch prototype.

CARIOCA test on the WPC is needed !!!

Positive and Negative Polarity

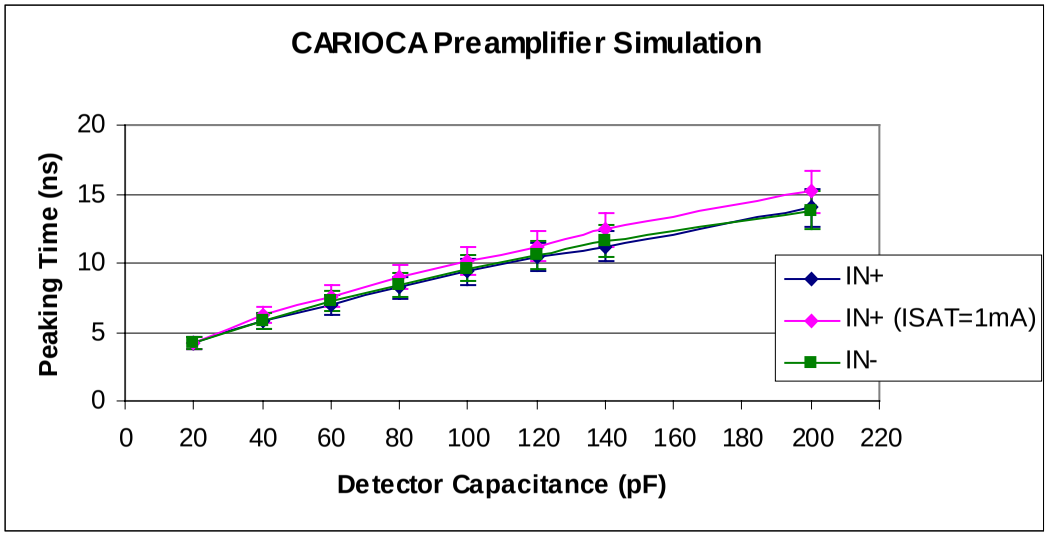


GOOD agreement within 10%

LHCb 2001-029

March 2001, D. Moraes et al.,

Test of CARIOCA chip prototype



FE-Architecture: Status

Overview of New Baseline Architecture:

LHCb 2001-030, March 2001, A. Lai et al., Update on Muon FE-Architecture

-> Realistic data flow between chambers and the Trigger/DAQ System

FE-boards

↓

(~10m)

-> (ASD-chip) -> digital signals (CARIOCA)

-> FE-control (DACs), Field Bus Node (DIALOG)

-> logical channel generation, delays, masking

~ 120-150 k phys. channels ~ 43k logical channels

~ 7-10k FE-boards

Intermediate boards

↓

(~4m)

-> logical ch. generation (final step for R3+R4)

~ 26k logical channels

168 Intermediate boards (was 1056)

Off Detector boards

-> Synchronization, Pipelines, Trigger interface

152 (168) ODE-boards

Channel Reduction

Details of Channel numbers:

Physical channels:

Physical channels	Station 1	Station 2	Station 3	Station 4	Station 5	Sum
Region 1 (wire pad)		144	144			288
Region 1 (cath pad)	1152	192	192	288	288	2112
Region 2 (wire pad)		288	288			576
Region 2 (cath pad)	2304	384	192	288	288	3456
Region 3	2304	1152	1152	576	576	5760
Region 4	2304	1152	1152	1152	1152	6912
Sum/Quad/Layer	8064	3312	3120	2304	2304	19104
Sum	64512	26496	24960	18432	18432	**152832**

Phys.ch. / log.pad (step 1):

Physical ch. / logical ch.	Station 1	Station 2	Station 3	Station 4	Station 5
Region 1 (wire pad)		1	1		
Region 1 (cath pad)	2	1	1	1	1
Region 2 (wire pad)		1	1		
Region 2 (cath pad)	4	4	2	1	1
Region 3	4	1	1	2	2
Region 4	4	1	1	4	4

Channels after Step 1 and 2:

ORed-Channels	Station 1	Station 2	Station 3	Station 4	Station 5	Sum
Region 1	576	336	336	288	288	1824
Region 2	576	384	384	288	288	1920
Region 3	576	1152	1152	288	288	3456
Region 4	576	1152	1152	288	288	3456
Sum/Quadrant	2304	3024	3024	1152	1152	10656
Sum	9216	12096	12096	4608	4608	**42624**

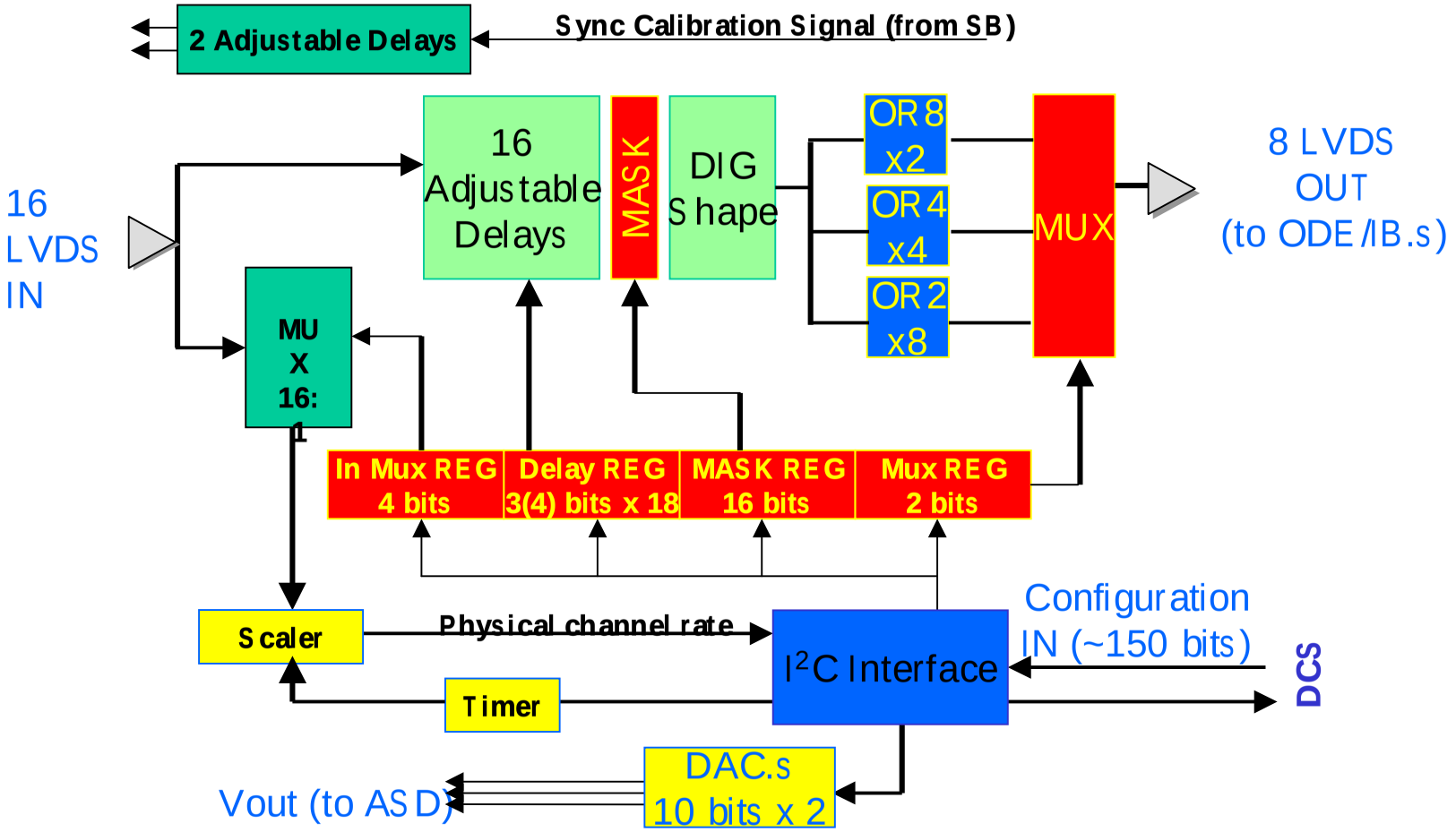
Logical channels:

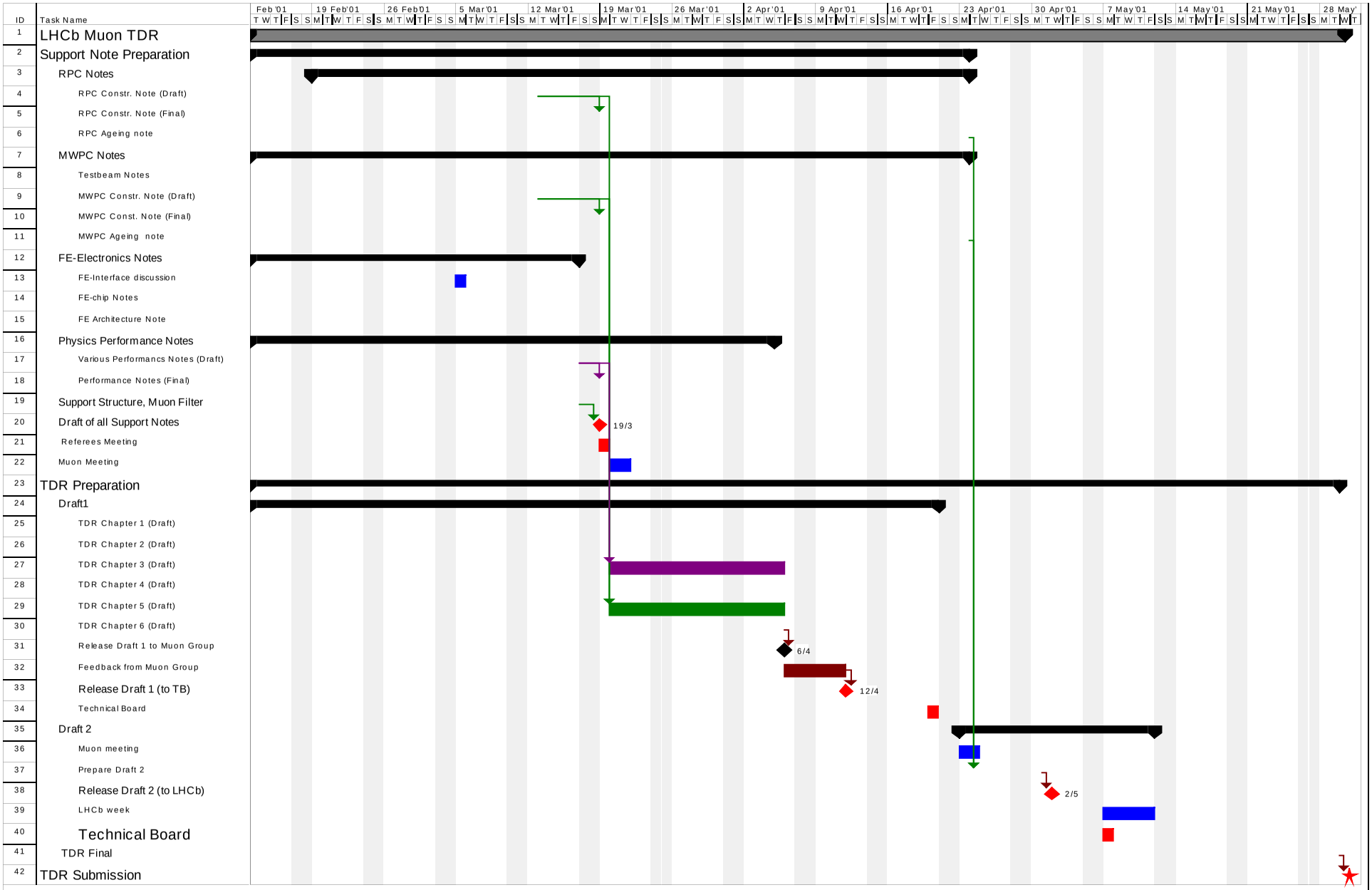
Number of Logical channels	Station 1	Station 2	Station 3	Station 4	Station 5	Sum
Region 1	576	336	336	288	288	1824
Region 2	576	384	384	168	168	1680
Region 3	576	336	336	120	120	1488
Region 4	576	336	336	120	120	1488
Sum/Quadrant	2304	1392	1392	696	696	6480
Sum	9216	5568	5568	2784	2784	**25920**

DIALOG

DIagnostics, time Adjuster and LOGics

(A.Cadeddu, A.Lai)




ID
Task Name
Feb '01
19 Feb'01
26 Feb'01
5 Mar'01
12 Mar'01
19 Mar'01
26 Mar '01
2 Apr'01
9 Apr'01
16 Apr'01
23 Apr'01
30 Apr'01
7 May'01
14 May'01
21 May'01
28 May'
1 LHCb Muon TDR
2 Support Note Preparation
3 RPC Notes
4 RPC Constr. Note (Draft)
5 RPC Constr. Note (Final)
6 RPC Ageing note
7 MWPC Notes
8 Testbeam Notes
9 MWPC Constr. Note (Draft)
10 MWPC Const. Note (Final)
11 MWPC Ageing note
12 FE-Electronics Notes
13 FE-Interface discussion
14 FE-chip Notes
15 FE Architecture Note
16 Physics Performance Notes
17 Various Performancs Notes (Draft)
18 Performance Notes (Final)
19 Support Structure, Muon Filter
20 Draft of all Support Notes
19/3
21 Referees Meeting
22 Muon Meeting
23 TDR Preparation
24 Draft1
25 TDR Chapter 1 (Draft)
26 TDR Chapter 2 (Draft)
27 TDR Chapter 3 (Draft)
28 TDR Chapter 4 (Draft)
29 TDR Chapter 5 (Draft)
30 TDR Chapter 6 (Draft)
31 Release Draft 1 to Muon Group
6/4
32 Feedback from Muon Group
33 Release Draft 1 (to TB)
12/4
34 Technical Board
35 Draft 2
36 Muon meeting
37 Prepare Draft 2
38 Release Draft 2 (to LHCb)
2/5
39 LHCb week
40 Technical Board
41 TDR Final
42 TDR Submission

Summary and Conclusions

- First results with realistic detector description and digitization are promising -> Detailed studies started
- More optimization work required for M1:
  - keep X_0 low (<10%)
  - At present 40% of total FE-channels in M1 due to high occupancy
- Good progress has been made towards a chamber design which is robust and simple. Ideas are evolving on chamber construction
- Performance of MWPC prototype according to expectations
  - Cross-talk between wire strips has to be understood better
- Promising results with triple GEM for M1 R1+R2
- Clear plan established for FE-chip development

  -> Schedule for CARIOCA is tight
- Optimized FE-Architecture more economic

Schedule for TDR tight, but we are progressing well