LHCb muon timing review

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Presentations and documentation: http://doc.cern.ch/age?a01530

A dedicated review of the muon timing alignment, and the implementation of the related SYNC TDC, was requested by the technical board after discussions on the muon TDR. The need for a dedicated TDC, for the muon detector, to be capable of performing correct timing synchronization to the LHC collisions, was not clearly understood by the TB members. The proposed implementation schedule for the dedicated SYNC TDC chip was also considered to be critical (DIALOG and Carioca ASIC's may also be critical).

The reviewers would like to congratulate the muon group for their thorough analysis of the timing synchronization problem in the muon detector. During the review it was clearly shown that the timing synchronization can be particularly difficult for the muon detector because of the low channel occupancy, the relatively high background from low energy particles, and the particular configuration of the muon detectors. The use of MWPC detectors with a rather large time jitter, caused by internal drift times, complicates the timing alignment for high occupancy regions. For low occupancy regions, using RPC detectors, the detector noise (assuming non oiled RPCs) is comparable to the real muon hits from the interactions.

A significant cost savings in the front-end electronics has been obtained by reducing the number of physical channels (120k) to a limited number of logical channels (26k). This, on the other hand, has made the timing alignment more delicate as each logical channel is made from a logic OR of signals from different detection layers and different chambers. The DIALOG chip (plus in some cases the Intermediate boards) takes care of performing the channel OR, and introduce programmable delays on each physical channel, to be capable of compensating for their individual time differences. This gives the means for making the correct time alignment, but also makes the adjustments of all these individual delays a significant task in obtaining correct timing synchronization.

From the presentations of the timing characteristics of the detector technologies used, it seems that the timing of detector channels, from the same physical chamber, can be considered to be the same within a few ns. This should be used, when possible, to simplify the readout electronics and timing calibration procedure. Variations over time, in the delays in the detectors and its analog front-end, caused by temperature, pressure, and high voltage drifts also seems to be sufficiently small, that it will not require timing

recalibrations within the expected working conditions. From this it is concluded that the timing of the muon detector can be expected to be relatively stable over time and that a complete recalibration of the detector timing only is needed during commissioning (and possibly once per year). Under normal running conditions, only marginal timing adjustments will be needed. However as it was pointed out by members of the muon group, a gain drift in one of the MWPC chambers (which would eventually result in a loss of efficiency) will be seen clearly as a drift in the time spectra. The reviewers agreed that this reinforce the usefulness of the TDC's for monitoring.

The time needed for collecting sufficient statistics for a (complete) time calibration is not considered critical, as such a recalibration is only needed in-frequently. It can be accepted to run for a day or two, at start up, to make a complete recalibration (if really needed). Bunch crossing synchronization is needed by all sub-detectors in LHCb and a special interaction trigger together with other features (consecutive triggers, no interactions in defined time windows before and after, etc., see LHCb note LHCb 2001-14, page 3 - 8) are centrally available to help with this task. Using the dedicated interaction trigger, on bunch collisions at the beginning of a bunch train, can significantly reduce the time needed to collect sufficient muon tracks. The defined L1 trigger accept rate of 40 kHz seems to be sufficient to use the DAQ system to collect and analyze event data during a timing calibration. At a 40 KHz L1 accept rate, 16 consecutive L0 triggers can be collected for every fifth LHC machine cycle. In case of only using a time window of a few consecutive L0 triggers (should in most cases be sufficient), data can be collected and analyzed for each LHC machine cycle. It is therefore felt that there is no specific needs to build special histogramming and processing features into the front-end electronics, to make this kind of data analysis. However a fast analysis of the data should be available in the DAQ in order to produce the proper delay adjustments within a few hours of data taking. The generation of histograms in the DAQ system can be built on real muon tracks, and the chambers used in the OR of the logical channels can be identified by tracking (except for the 2 layers).

It was clearly demonstrated that the availability of TDC data, to build detailed timing histograms per channel (possible for both logical and physical channels by using masking during special timing calibration runs), is extremely useful for timing calibration and continuous detector monitoring. A possible scheme to perform accurate time alignment without TDC information was not given, but the reviewers though felt, that it can probably be made to work, when time differences between channels from the same chamber are insignificant. The availability of TDC information clearly gives a significant advantage in the running of the detector, and it is a highly recommended option to implement, if it can be shown not to have a significant negative impact on the time schedule of the implementation of the muon electronics.

The option of having TDC data available only for a limited number of channels (one or few per ODE with a programmable selection of channel) should be considered as a backup solution. In this case an existing TDC can be used (F1, HPTDC or alike) and the remaining readout part can be made with (antifuse) FPGA's and discreet memories.

In the planning given in the muon TDR, the implementation of the SYNC chip appear as one of the critical components (together with the Carioca and Dialog ASIC). A full electronics chain test is proposed for the summer 2002 and a full SYNC chip (ASIC) can not be made available within such a short time frame. The design work on the SYNC ASIC will only start at the beginning of 2002 assuming that the Dialog chip is successfully completed by then (design team currently working on the Dialog chip). A complete SYNC ASIC can therefore not be expected to be available before the beginning of 2003. To have something ready for the electronics test in the summer of 2002, the muon group proposes to make a first test with a simplified SYNC implemented in a FPGA. The FPGA SYNC can be considered as a first prototype that can then be mapped into a real ASIC.

The proposed implementation of the SYNC TDC has the same basic functions as seen in the OTIS TDC, currently under development in Heidelberg for the LHCb outer tracker. This development is in a more advanced stage, as prototypes have already made and tested. It is highly encouraged that a collaboration between the SYNC and OTIS is made, and if possible merged into a common effort. This will bring significant advantages to both the muon and the outer tracker project. Both detectors rely heavily on the availability of such a TDC. The major difference from the OTIS to the SYNC seems to be the synchronized outputs needed by the muon trigger. Such a simple synchronization stage can though be made in a separate FPGA (antifuse), as the detector data at this point is supposed to have been time aligned by the DIALOG chip. This FPGA can also be used to format data to be sent on the optical links, to the muon trigger electronics located in the counting room. By making the data path to the muon trigger "independent" of the data path to the readout, the two parts can easier be made by two independent groups, and it gives more flexibility for the implementation of a TDC for the readout (possible use of OTIS or other TDC).

In case that more detailed investigations finds that TDC data is not required (or only on a few channels), most of the functions (L0 and L1 buffering) of the ODE can be moved to the counting room. All binary detector data is already available in the counting room on the muon trigger optical links. The complete readout can in this case be implemented on the muon trigger cards (if sufficient space is available) or on independent readout cards using optical splitters. Moving as much as possible of the front-end electronics out of the cavern, with radiation and magnetic fields, will have significant advantages for the accessibility and reliability of the front-end electronics. Such a scenario will only require simple interface cards in the cavern, with the optical link interfaces and possibly a few TDC channels.

As a summary of the review it can be concluded that:

- Channels from the same physical chamber can be considered to have sufficiently similar timing, that this can be used to simplify the timing alignment procedure.
- The L1 rate is sufficiently high to perform timing alignment processing in the DAQ system, therefore no histogramming is needed in the front-end.

- The availability of TDC measurements is extremely useful for the commissioning, timing calibration and monitoring of the muon detector.
- The availability of TDC information from a limited number of channels seems sufficient (programmable selection of channel) for timing alignment and detector monitoring.
- The implementation of the SYNC ASIC (and also Dialog and Carioca ASIC's) is on the critical path of the time schedule of the muon electronics. Problems in ASIC implementations have in many cases been seen to give significant delays in the implementation of electronics for HEP experiments, and should therefore be looked at and monitored closely.
- The data synchronization for the muon trigger seems sufficiently simple, that it can be performed in a separate (antifuse) FPGA. This FPGA can also perform data formatting and interfacing to the optical links.
- If TDC information is only needed on a limited number of channels (or not at all) the majority of the functions on the ODE can be moved into the counting room using the binary data available on the optical muon trigger links.

The following recommendations can be made:

- Make a first implementation of the basic SYNC functionality in a FPGA for the system tests for summer 2002.
- Collaboration between the SYNC and the OTIS is highly encouraged. Discussions between the OTIS and the SYNC designers must be started as quickly as possible to determine if a common development can be made. If it is still found that a special SYNC development is needed, it will be advantageous to use the same technology as the OTIS (and also the new sub-micron DTMROC for the ATLAS TRT) to use existing building blocks (DLL, memories, etc).
- The muon group should determine if it will be advantageous to have the synchronization of the muon trigger data in a separate FPGA (makes the two paths more independent and allows the use of alternative TDC's).
- Despite the strong veto of the muon group to discuss the possibility of moving the ODE into the counting room, it is recommended to study this option for reasons of reliability, accessibility and maintenance. The muon group must be aware that special requirements to the immunity to radiation effects will be enforced. Extensive verifications and testing of electronics for radiation environments are known to be time consuming and expensive.