The Service Board system

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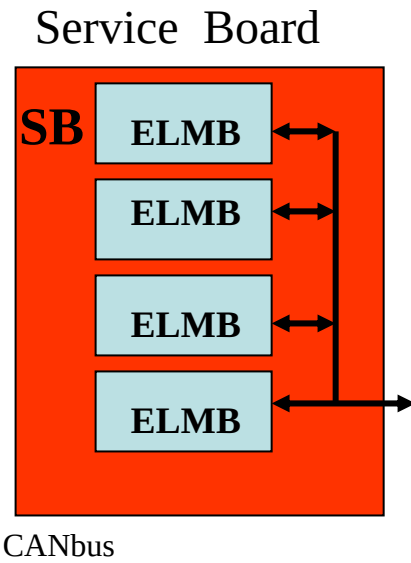
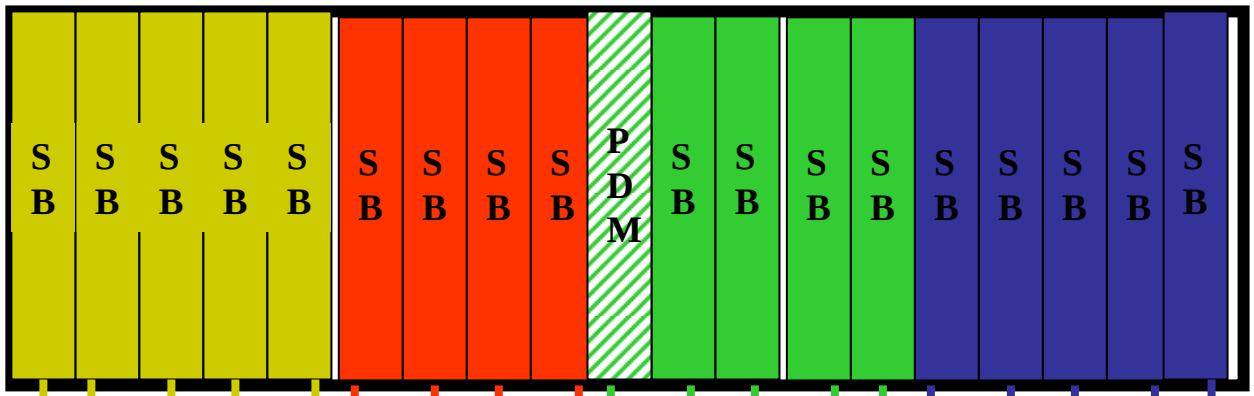
Service Board System





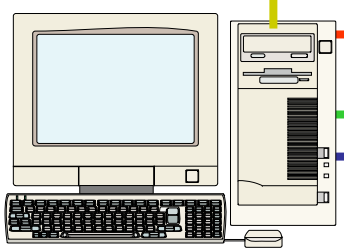
Custom Backplane

17 Can nodes

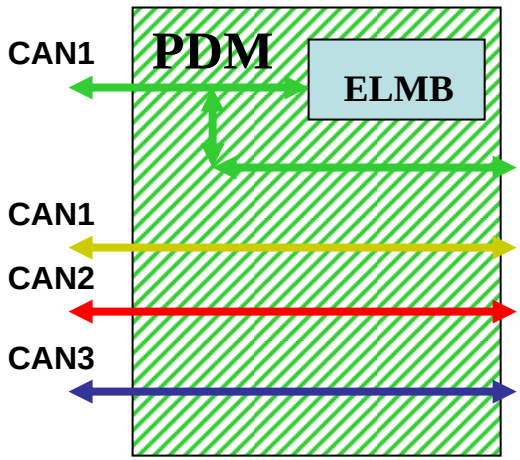
16 Can nodes

17 Can nodes

17 Can nodes

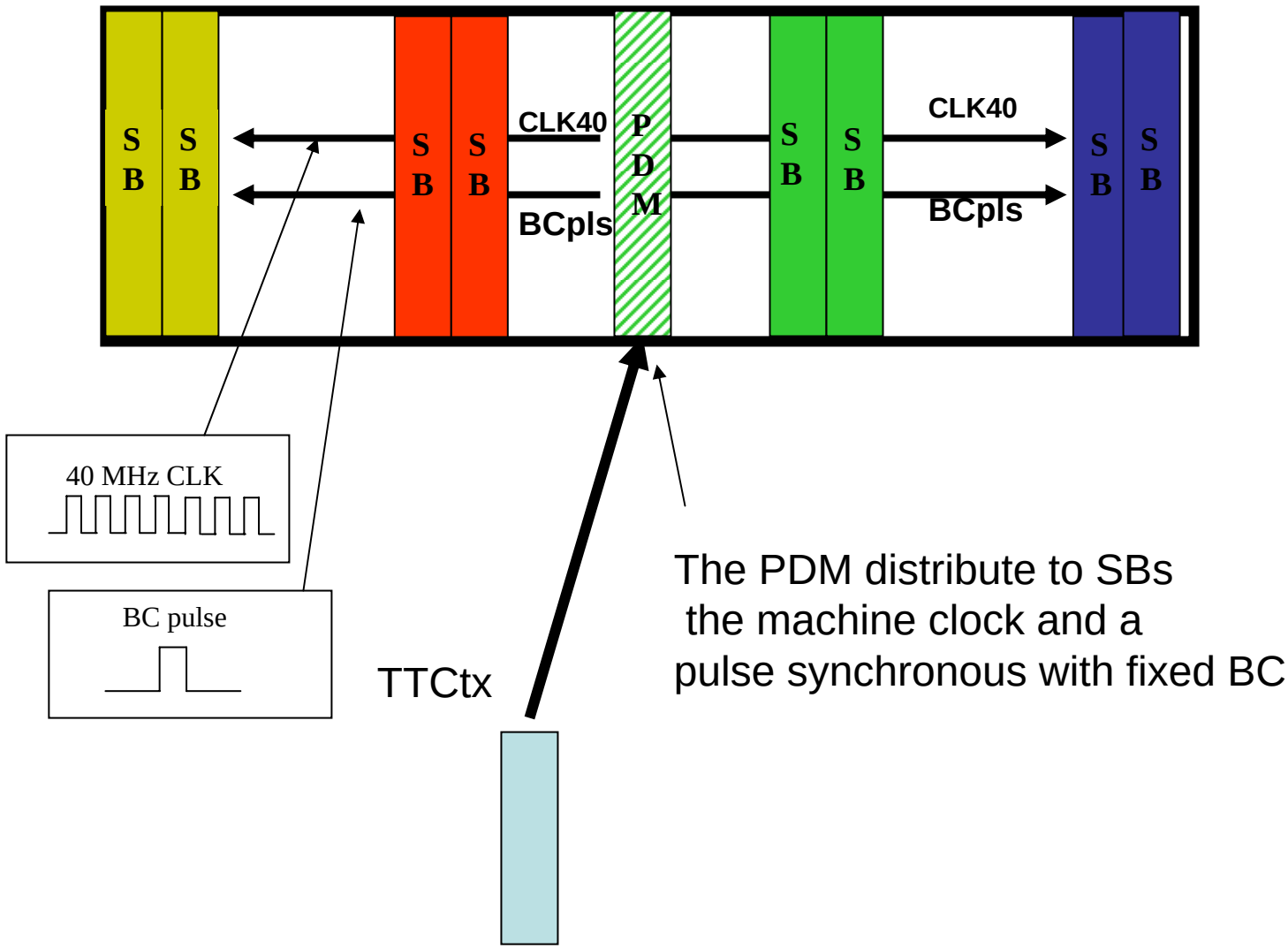


Pulse Distributor Module



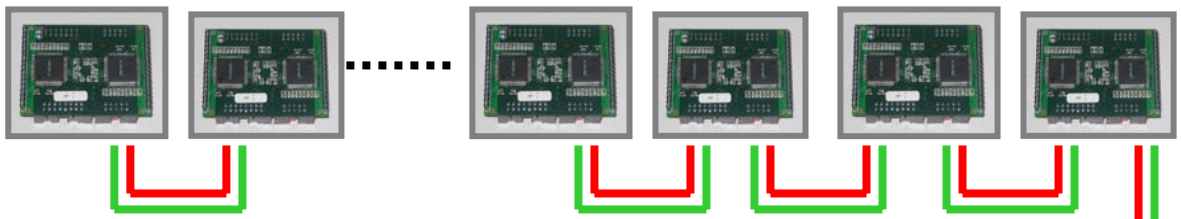
System numbers:
10 Crates
156 Service Board
10 PDM
40 CANbus Branch

Machine Clock and BC pulse distribution



FEB control and pulse distribution

Up to 8 Cardiac Board for each lvds i2c branch



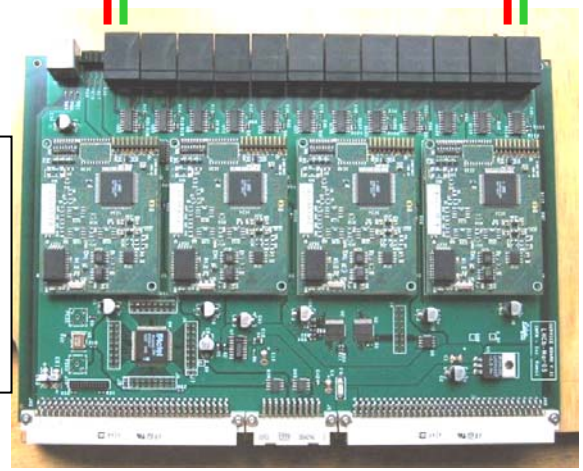
12 x (I2C+TST signal)

I2c LVDS signals:SCL,SDAin,SDAout

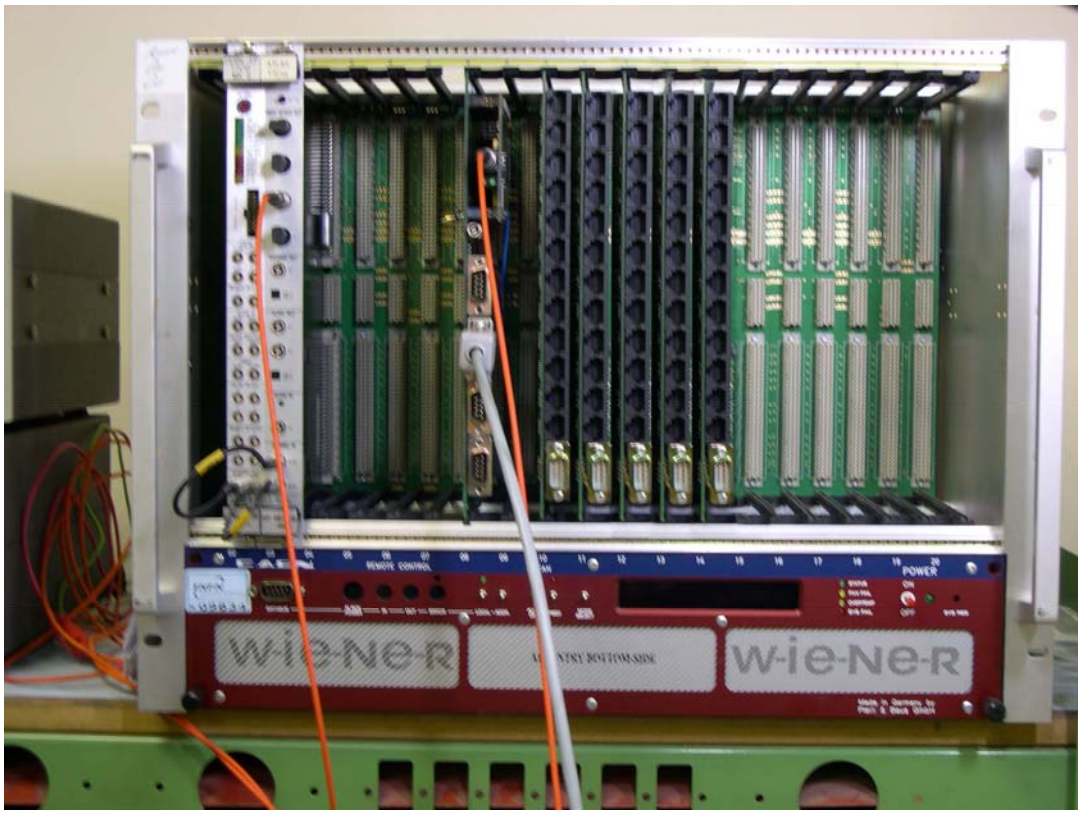
LVDS TST pulse,TTL Reset

Read Write Dialog Registers

Send pulse to measure rate,
calibrate DLL,sync pulse, RESET FEB



Service Board Lab Crate

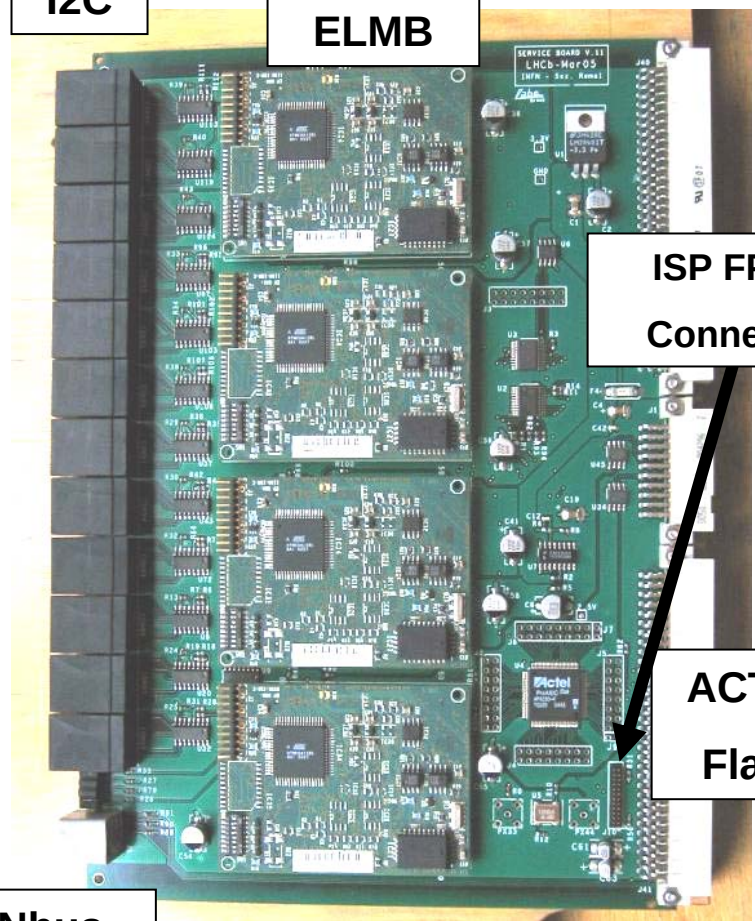


Feb 2005

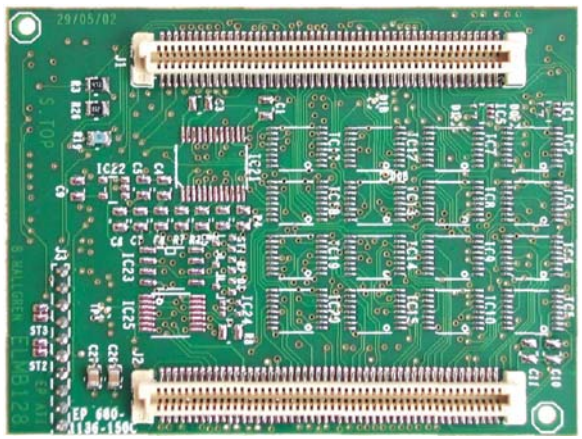
Service Board

(Ten preproduction Boards)

- **Service Boards**
  - Program firmware via CANbus
    - One ELMB
    - All ELMBs
  - New Features in the ELMB Firmware
    - Address >>> Crate Slot position
    - Scan for DIALOGs (PDO)
  - New Flash ACTEL with new features
    - ELMB Reset
    - PDM Reset
    - Tst Pulse logic with pre-scaler (DIALOG testing)
    - Synchronous i2c slave state machine



ELMB128 ATmega128



AVR RISC architecture ATMEL ATmega128

- 0.35 µm technology instead of 0.5 µm
- 128 kbytes of on-chip flash memory,
- 4 kbytes of SRAM
- 4 kbytes of EEPROM.
- In-System Programming via CAN bus using ATmega128 Boot code.

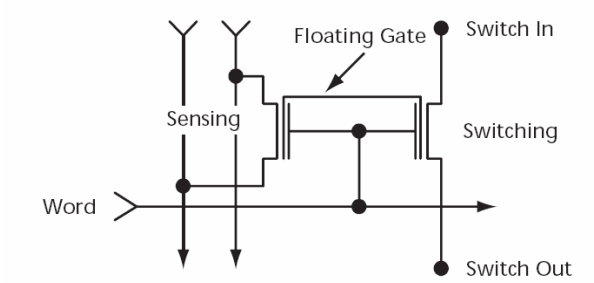
Peripheral Features

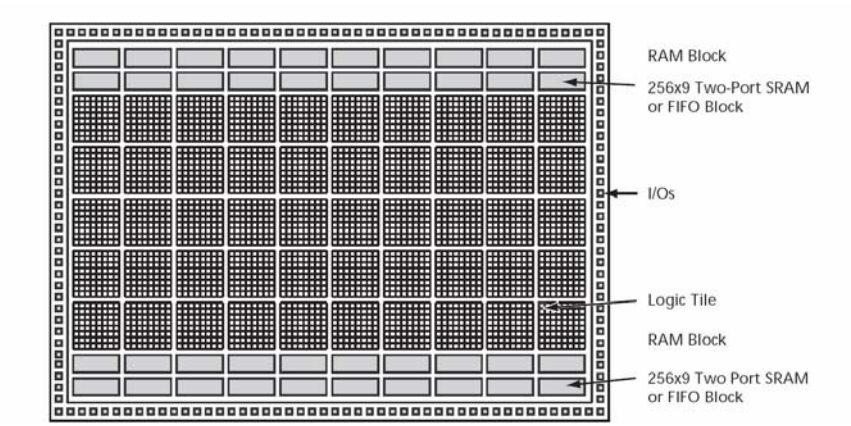
- Full CAN controller interface with PCA82C250

I/O lines available

- 18 digital bi-directional I/O lines , 8 digital output lines ,8 digitial inputs or analog inputs with adc

ProASIC^{PLUS} Flash Family FPGAs





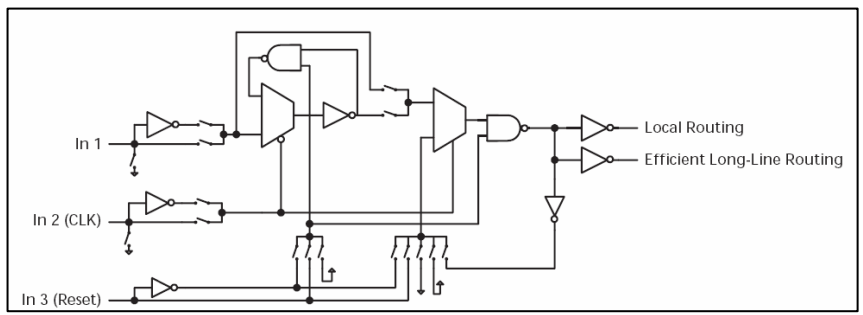
Commercial and Industrial

- 3072- 56320 Tile
- 27 k to 198 kbits of Two-Port SRAM
- 66 to 712 User I/Os

Tile

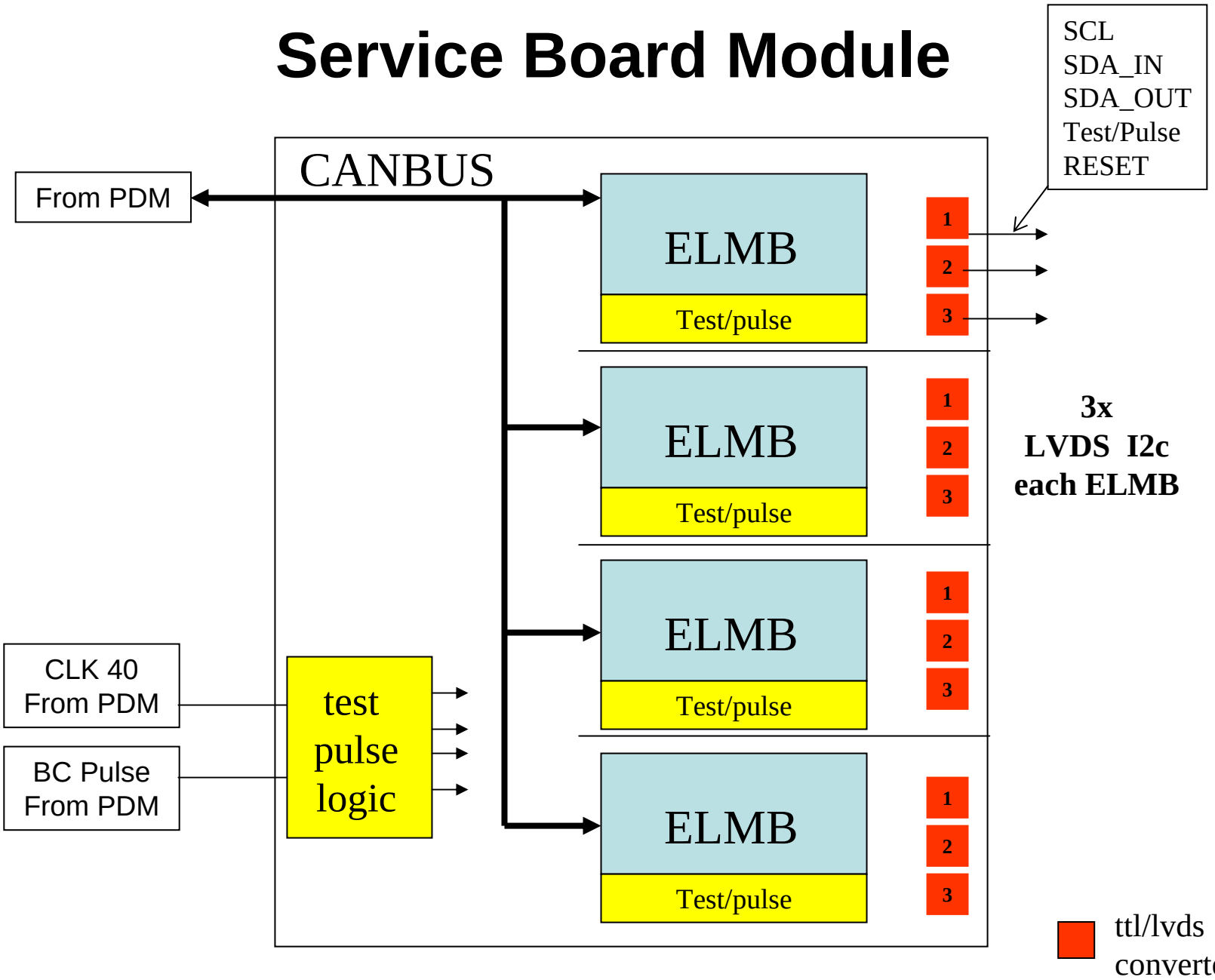
Reprogrammable Flash Technology

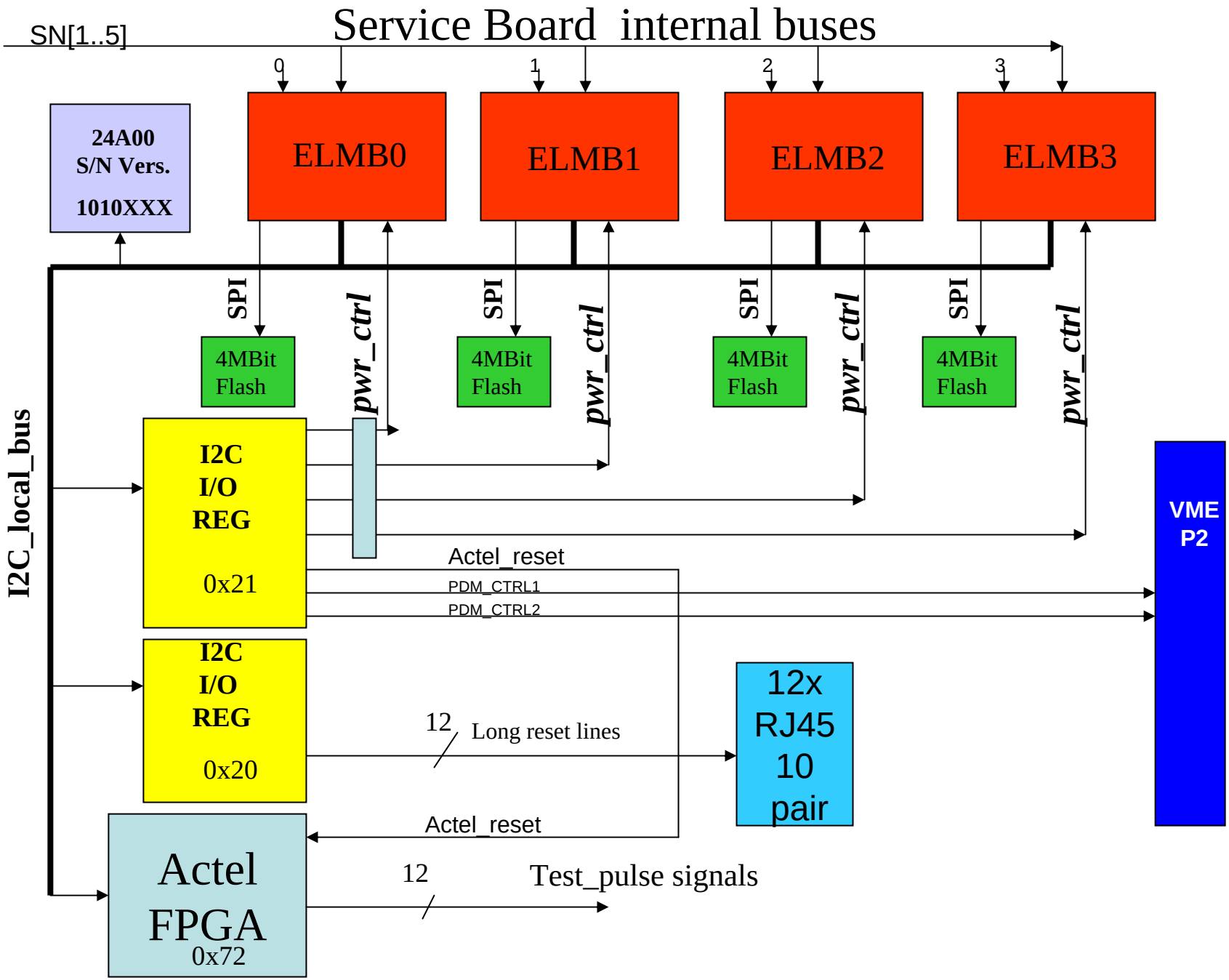
- 0.22 µ 4 LM Flash-Based CMOS Process
- Live at Power-Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Up Cycles

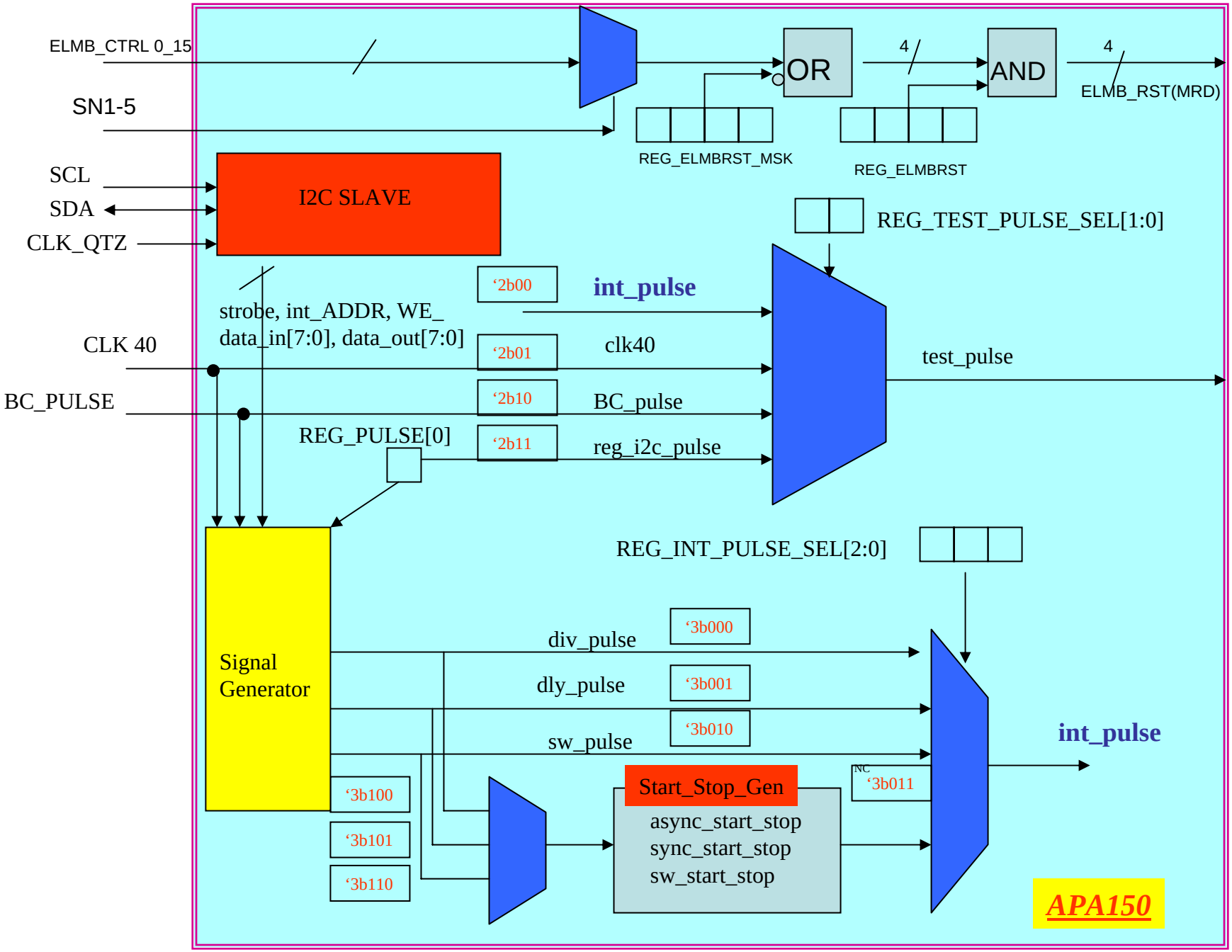


Radiation Tolerant,Flash Cell SEU immune

Service Board Module



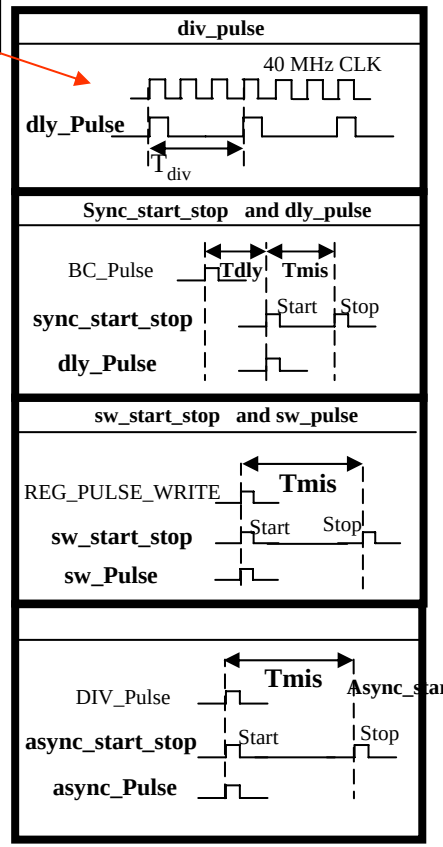

Service Board internal buses
SN[1..5]
0
1
2
3
24A00
S/N Vers.
1010XXX
ELMB0
ELMB1
ELMB2
ELMB3
SPI
pwr_ctrl
4MBit
Flash
I2C_local_bus
I2C
I/O
REG
0x21
I2C
I/O
REG
0x20
Actel_reset
PDM_CTRL1
PDM_CTRL2
12
Long reset lines
12x
RJ45
10
pair
VME
P2
Actel_reset
Actel
FPGA
0x72
12
Test_pulse signals


ELMB_CTRL 0_15
SN1-5
OR
4
AND
4
ELMB_RST(MRD)
REG_ELMBRST_MSK
REG_ELMBRST
SCL
SDA
CLK_QTZ
I2C SLAVE
REG_TEST_PULSE_SEL[1:0]
'2b00
int_pulse
strobe, int_ADDR, WE_
data_in[7:0], data_out[7:0]
CLK 40
'2b01
clk40
test_pulse
BC_PULSE
'2b10
BC_pulse
REG_PULSE[0]
'2b11
reg_i2c_pulse
REG_INT_PULSE_SEL[2:0]
Signal
Generator
'3b000
div_pulse
dly_pulse
'3b001
'3b010
sw_pulse
int_pulse
'3b100
'3b101
'3b110
Start_Stop_Gen
async_start_stop
sync_start_stop
sw_start_stop
NC
'3b011
APA150

SB & DIALOG Control

- **Control of all DIALOG registers**
  - Threshold
  - Pattern Pulse Generation
  - Scaler
  - …

Pre-scaler

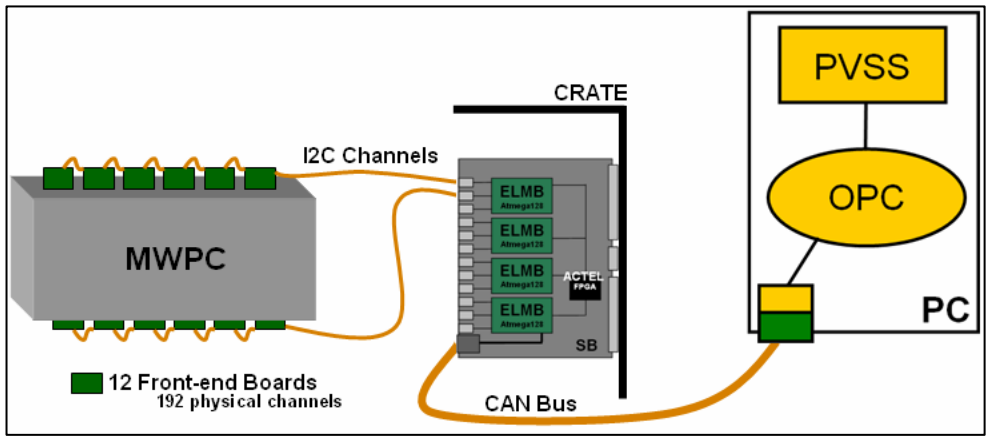


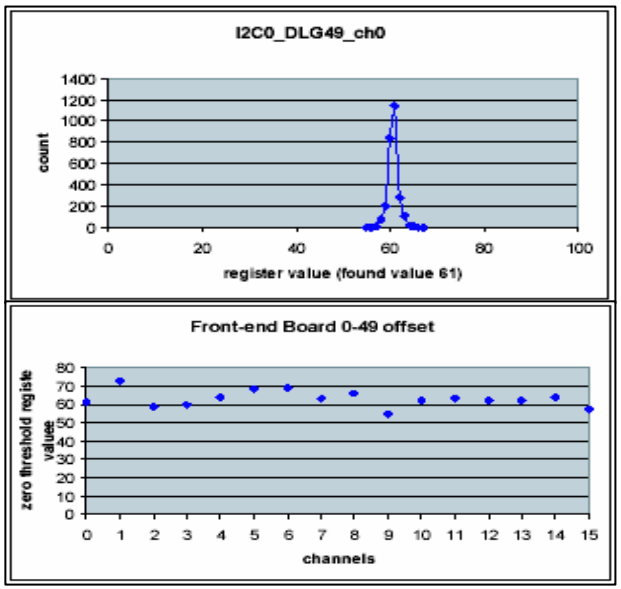
- **Access to ACTEL (FPGA) registers**
  - Test Pulse
    - 40 MHz
    - div_pulse
    - delay_pulse
    - sw_start_stop
    - ...
  - Reset ELMB
  - Mask for Test Pulse

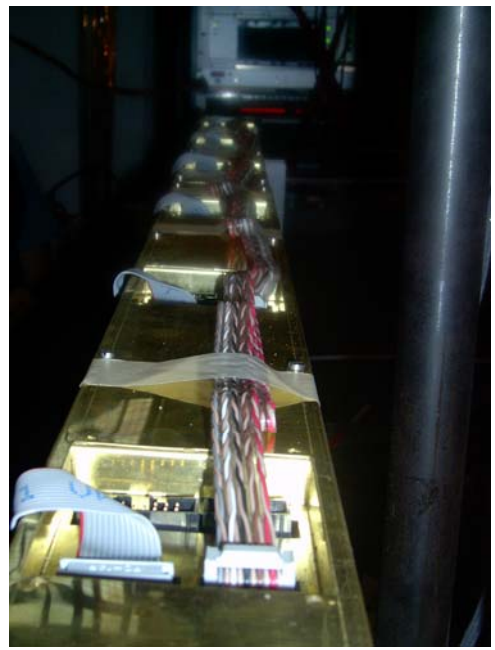
Test Using GIF Facilities (July 2004)

Test of Frascati MWPC Chamber

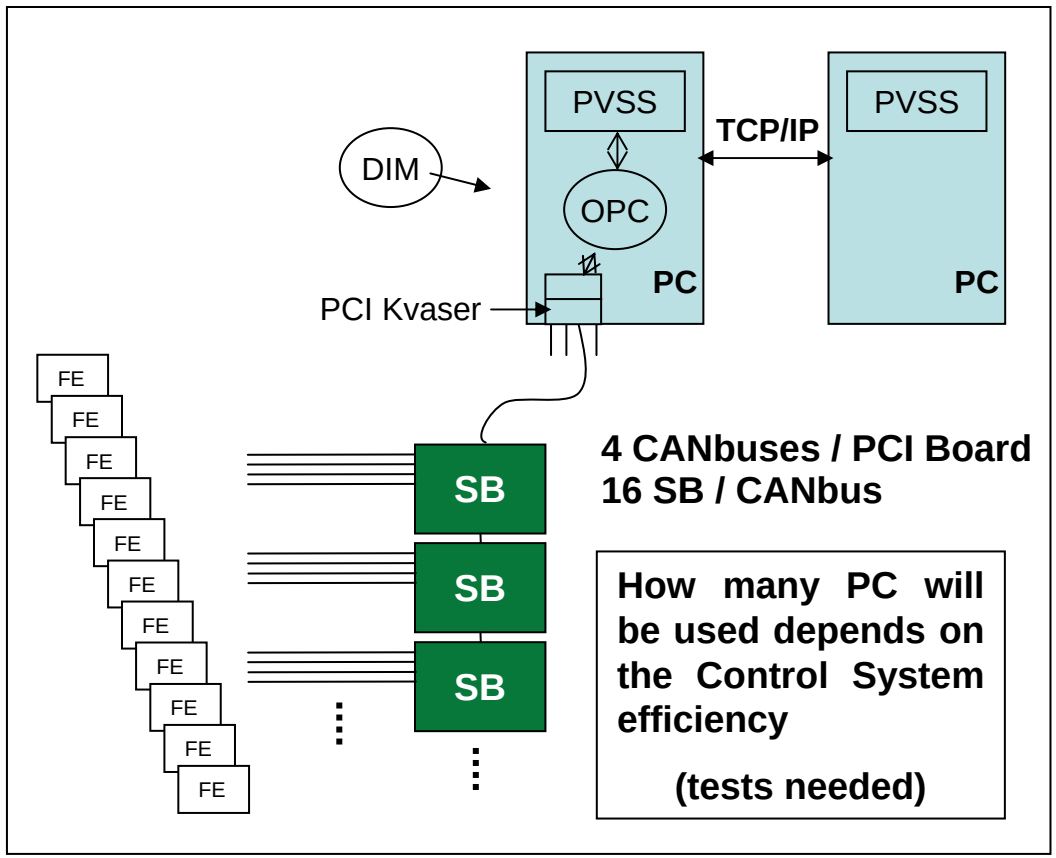
- 192 channels (12 FEBs)
- Control of all registes – ok
- Calibration of all channels – ok
- Reset Ctrl – needed and implemented

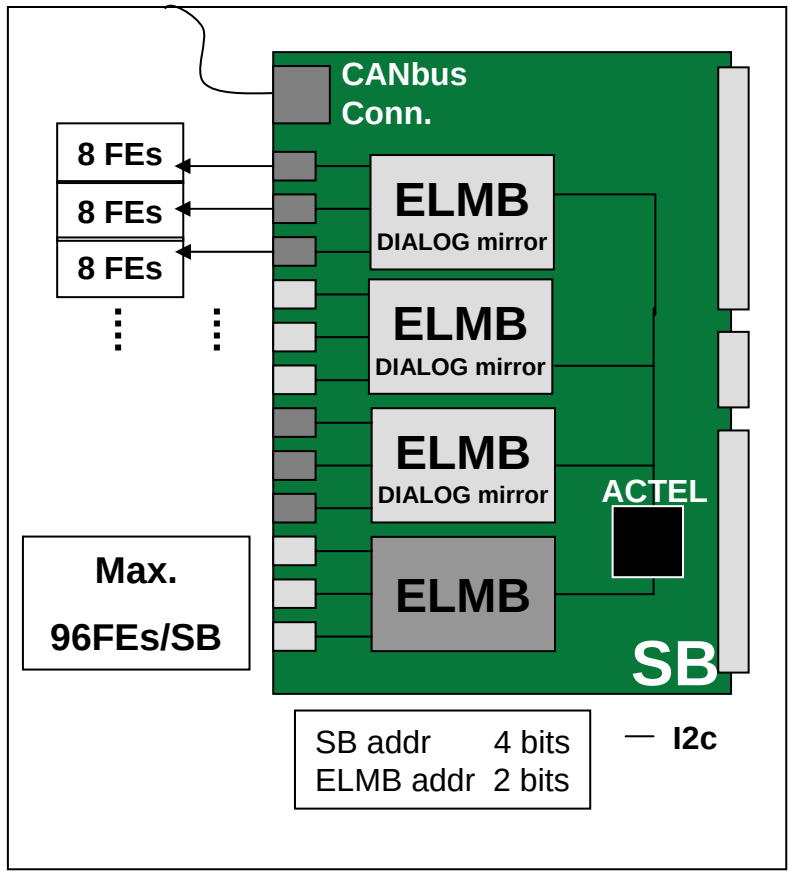






Control System Overview

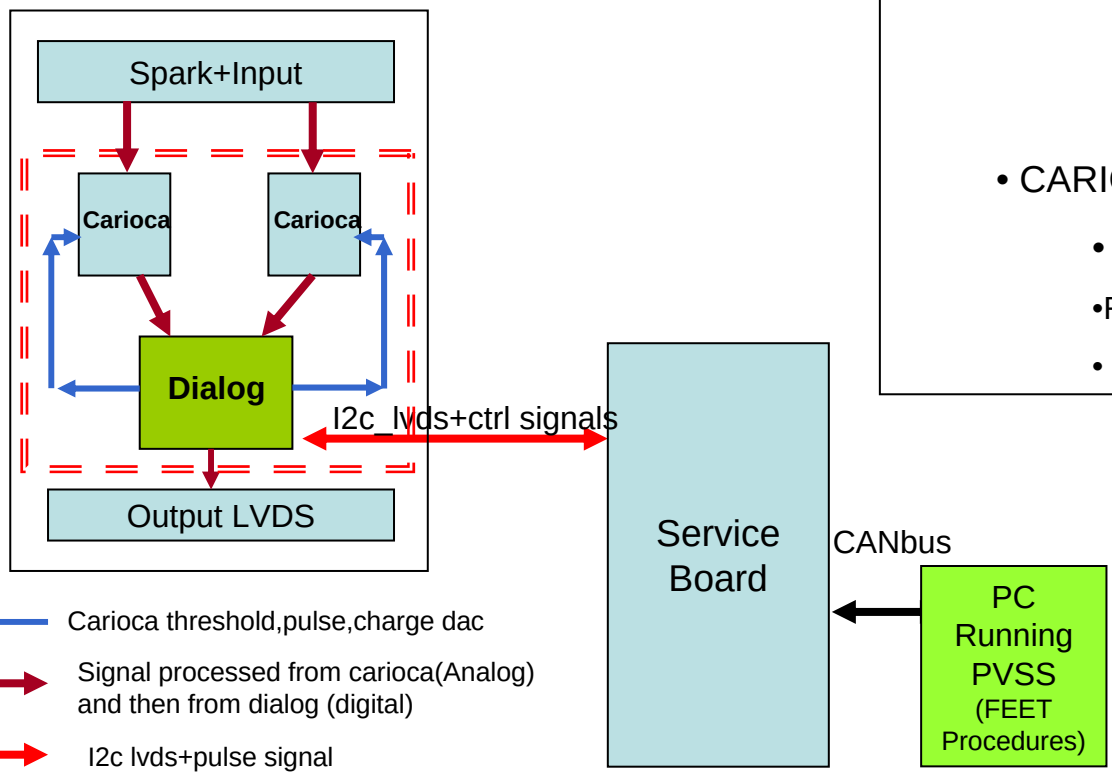




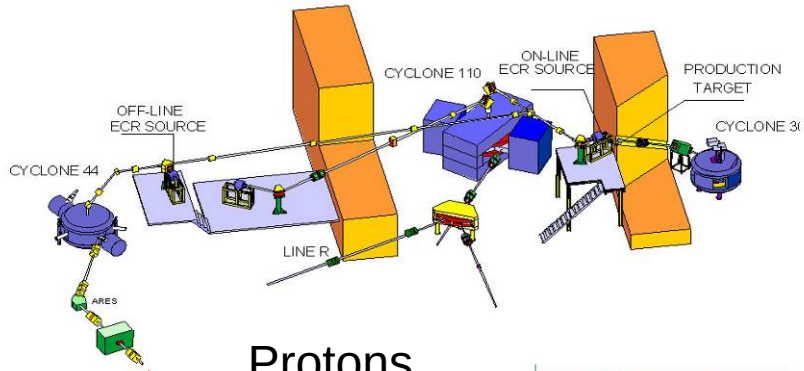
SB Front-end Testing

- **i2c lvds + ctrl signals**
  - SCL
  - SDA_IN
  - SDA_OUT
  - Test Pulse
  - RESET

- **CARDIAC Test**
  - DIALOG Functionality
    - Threshold
    - Pulse Generator
    - Test Dialog Channels
      - Pattern Generator
      - Scaler
      - Tst Pulse
      - ...
  - CARIOCA Test
    - If all channels are responding
    - Rate Method (?)
    - …



Voltage regulators test



Protons
60 MeV

CRC

Power Supply

1 m

Rad Area

LP2953
Or
LM3940
Board

Ethernet

RS232

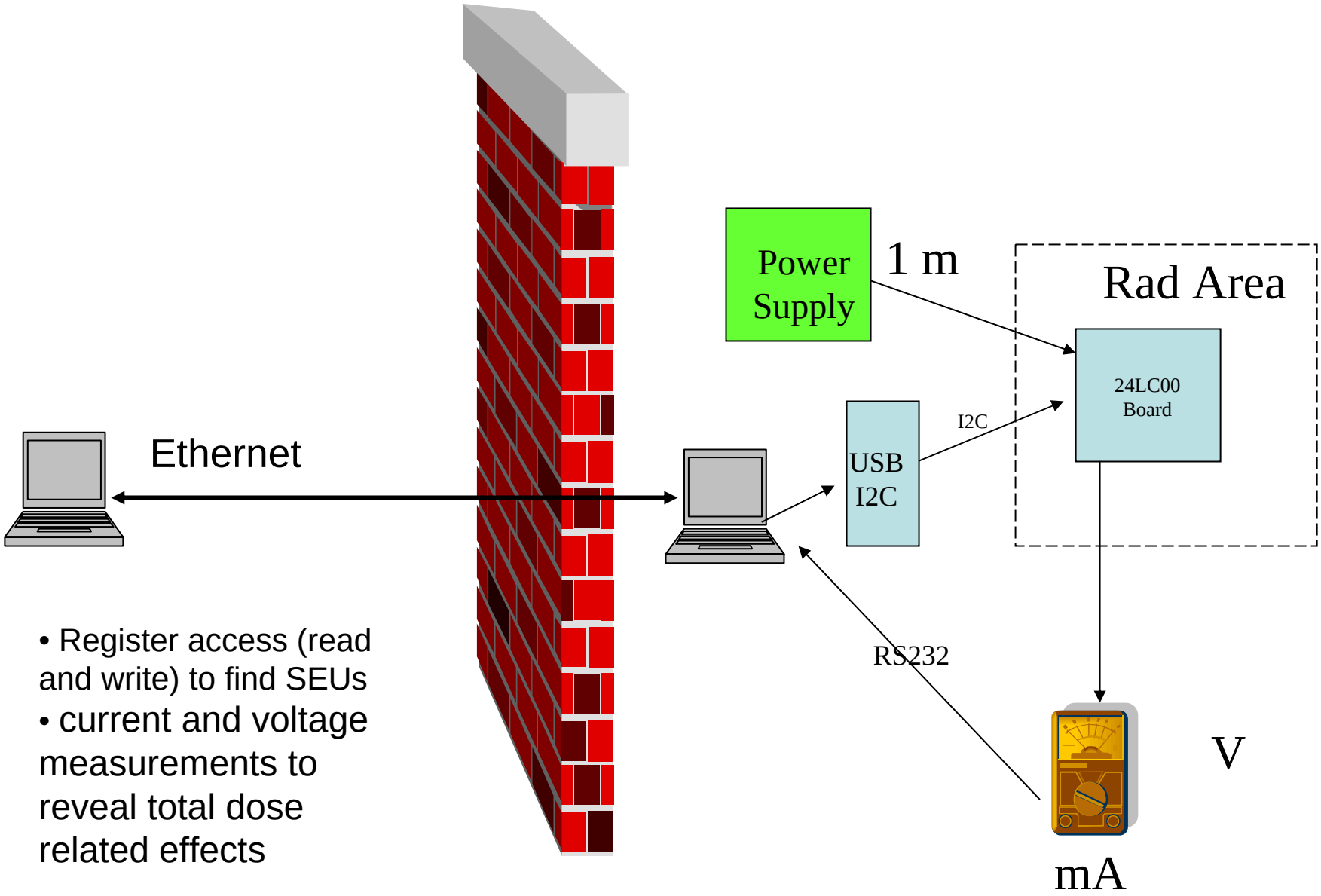
RS232

V

mA

- Data logging of current and voltage measurements to reveal SEU and total dose related effects

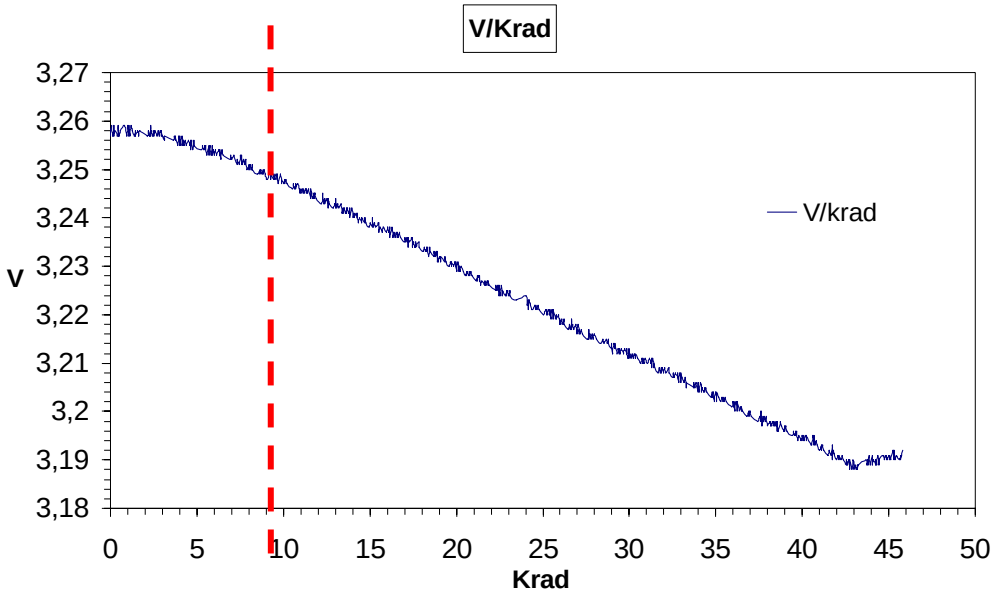
Flash memory test

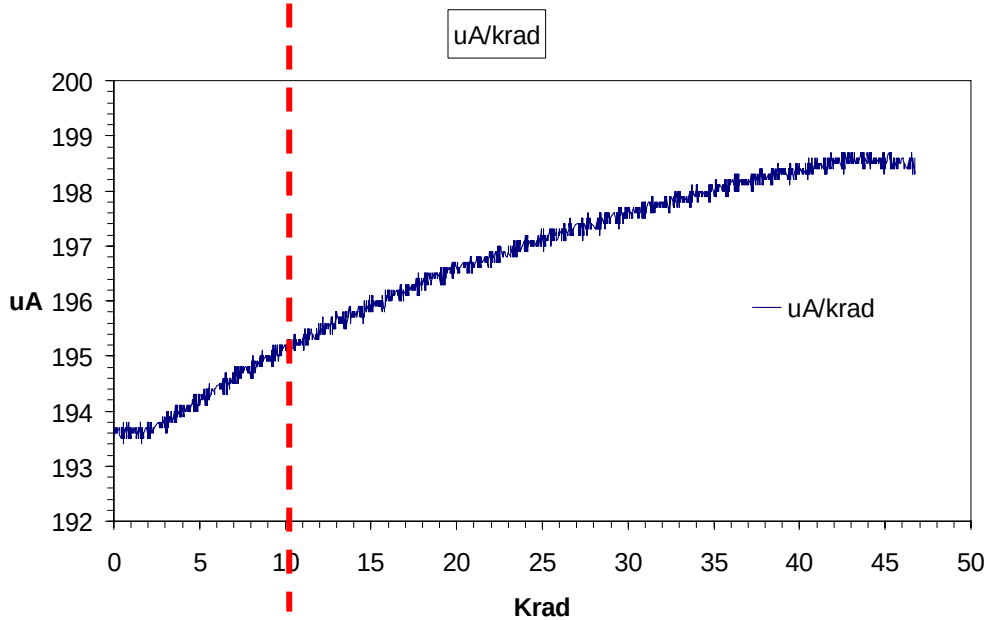


- Register access (read and write) to find SEUs
- current and voltage measurements to reveal total dose related effects

LM3940: 3.3 V output voltage regulator

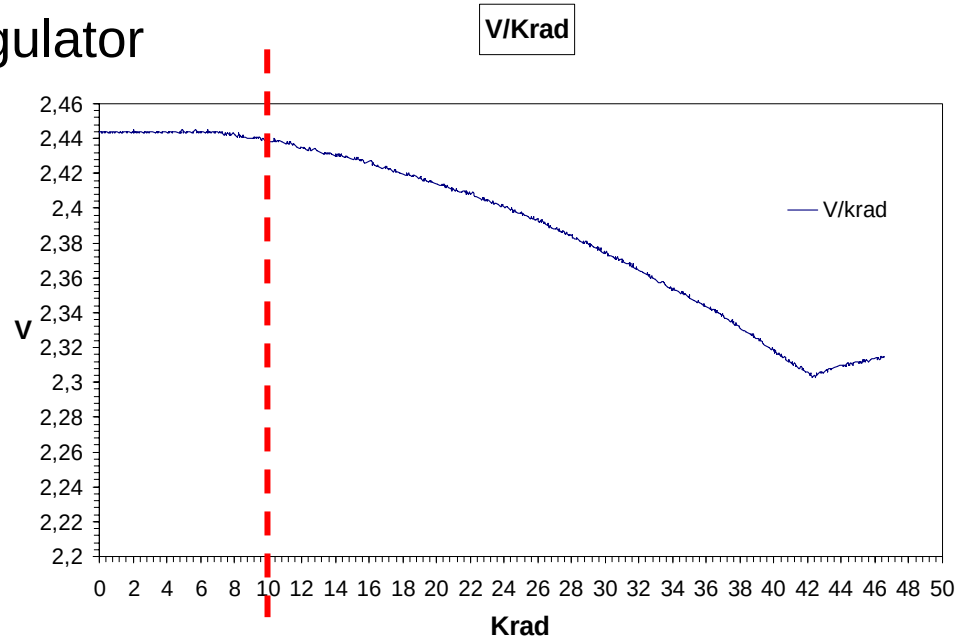
- **Tests: ok**
- No voltage and current peaks
- Voltage within operating range
- Current variations below 2uA
- Device break-point well beyond 10Krad

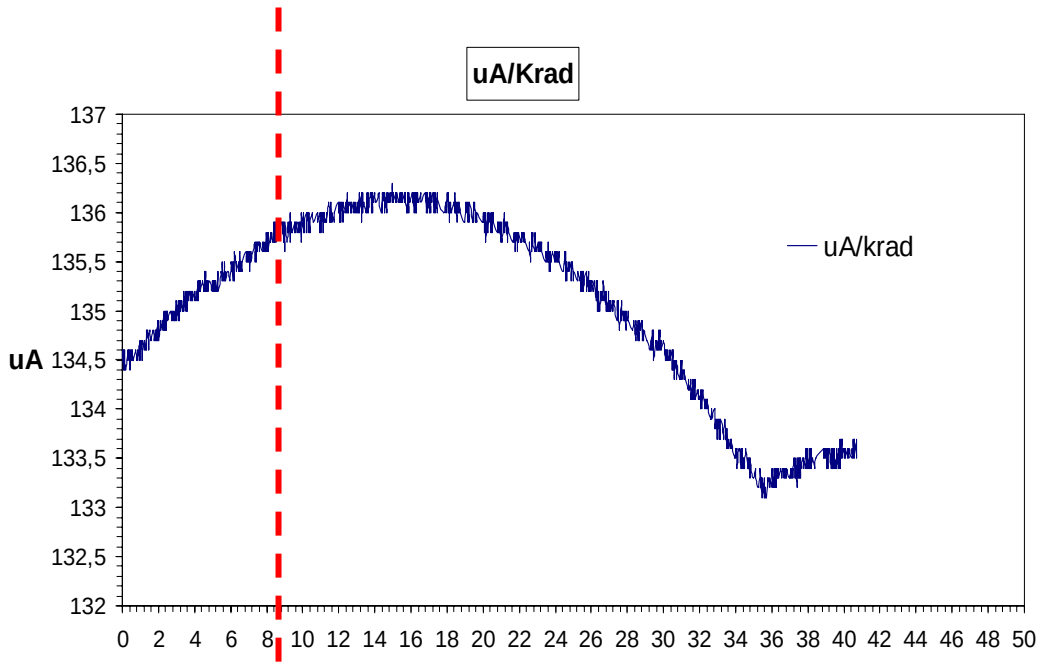




LP2953 : 2.5 V output voltage regulator

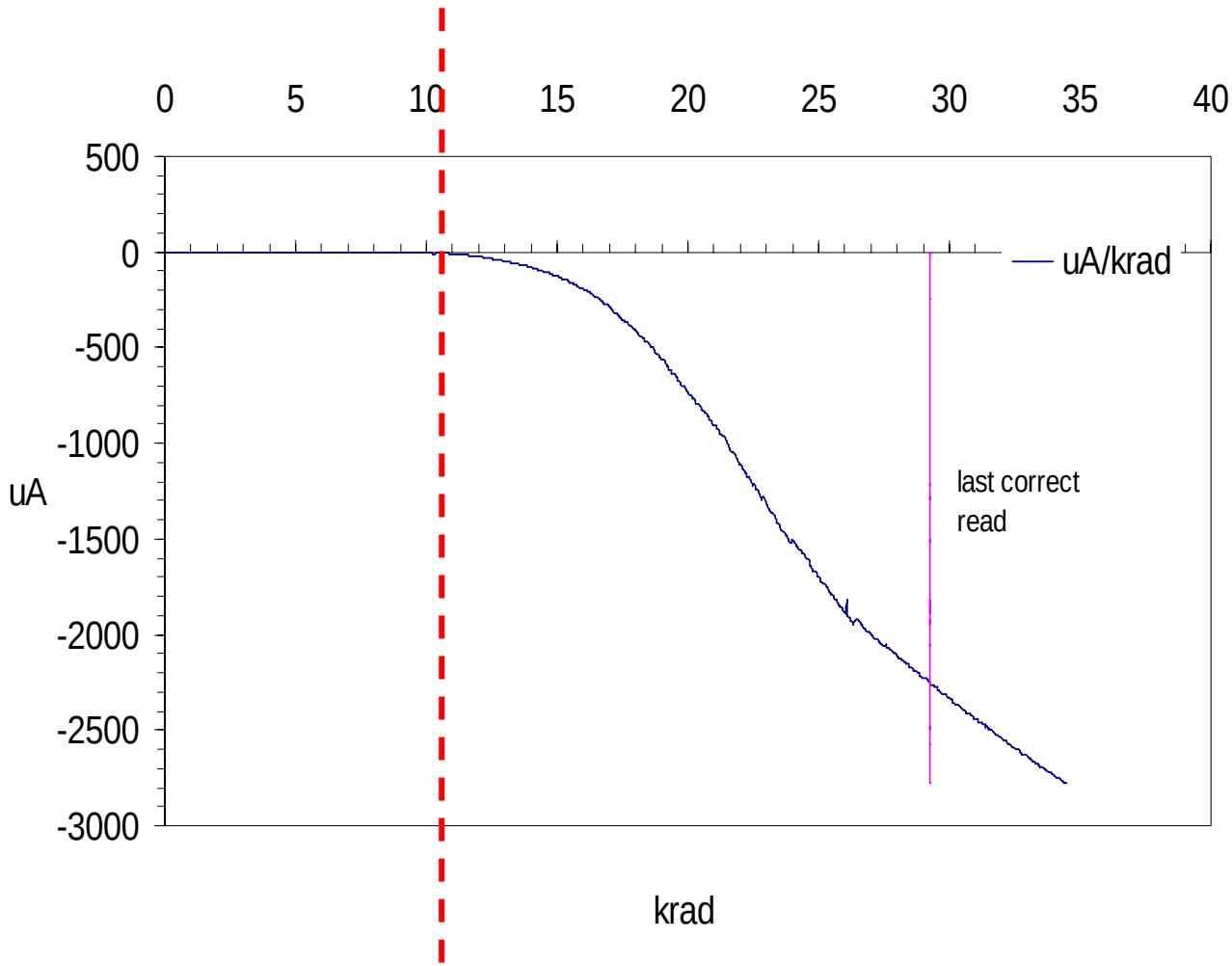
- **Tests: ok**
- No voltage and current peaks
- Voltage within operating range
- Current variations below 2uA
- Device break-point well beyond 10Krad





24LC00 :128 Bit Flash PROM

- No SEU found
- Reliable operation up to ~30Krad equiv.
- No issues for foreseeable total dose values (<10Krad)

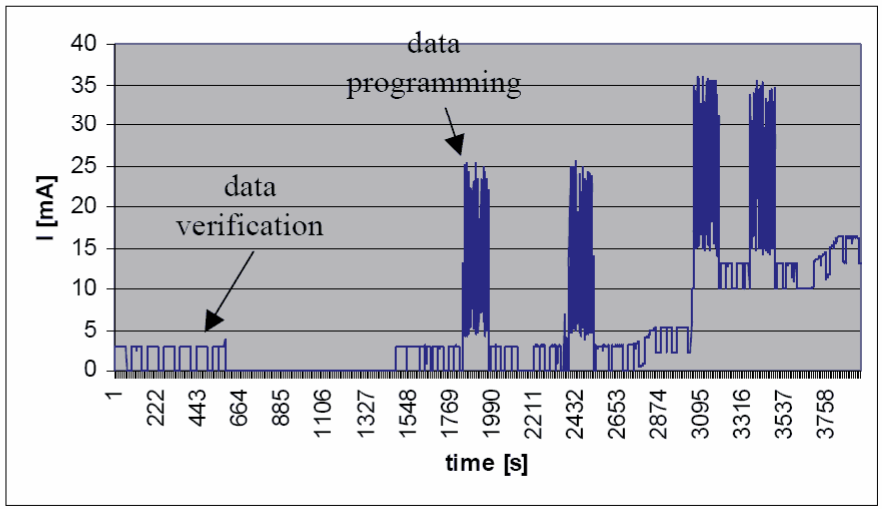


Atmel Flash SEE Test

- Flux applied: $5 \cdot 10^8$ h/cm^2/s
- Fluence: $2 \cdot 10^{11}$ h/cm^2
- The chip was monitored during data programming and verification (0101... pattern was used)
- No errors on flash memory
- 83, 83, 38, 56 bit errors on each of the RAMs after the applied fluence
- Power consumption increase due to total dose effects
- For a bigger fluence the serial interface stopped working correctly.

AT45DB041B features:
- 3.3 V
- serial interface flash memory
- SPI compatible
- 4,325,376 bits of memory
- two 264-byte SRAM data buffers

RESULTS:
- 4 chips tested
- Flash soft $SEU_f < 6.8 \cdot 10^{-9}$ s^{-1}
- RAM soft $SEU_f = 5.6 \cdot 10^{-7}$ s^{-1}
- $2 \cdot 10^{11}$ h/cm^2 ~ $2 \cdot 14$ krad = 28 krad

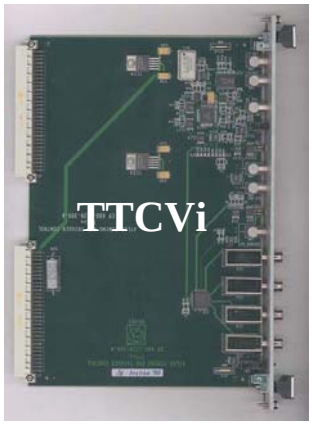


PDM

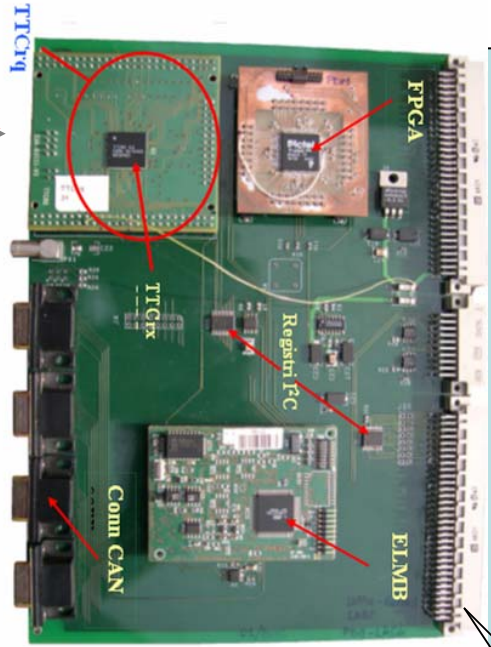
Pulse Distribution Module

- Distribute CANbus to Backplane
- Receive the timing information form TTCtx
- Distribute Machine Clock
- Produce a pulse synchronous with specified BC number
- An ELMB setting up TTCrx ,PDM FPGA,Reset hanging SB

Pulse Distribution Module



TTC
Fiber



Custom Backplane

4 nodi
CANBUS

Clk40

bc_pulse

PDM_RST

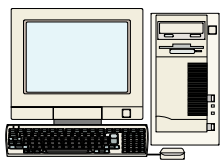
PDM_SHTDWN

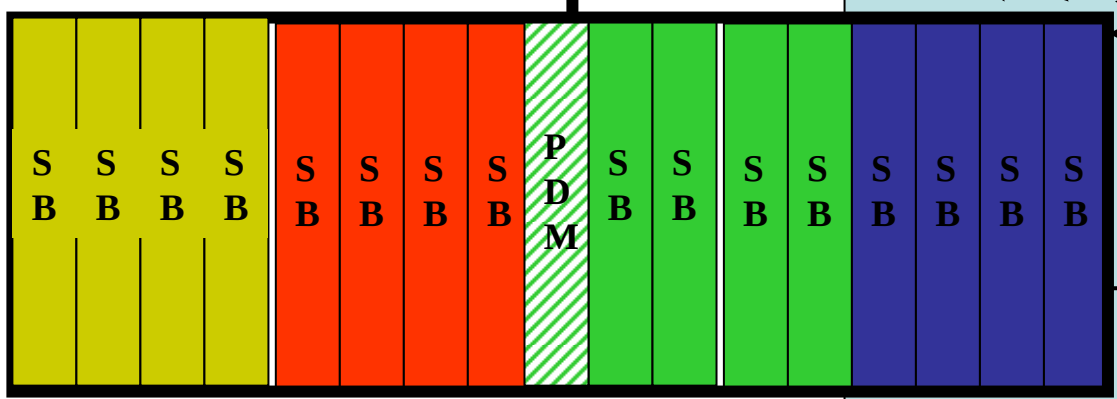
SB_RESET

4CANBUS
Nodes

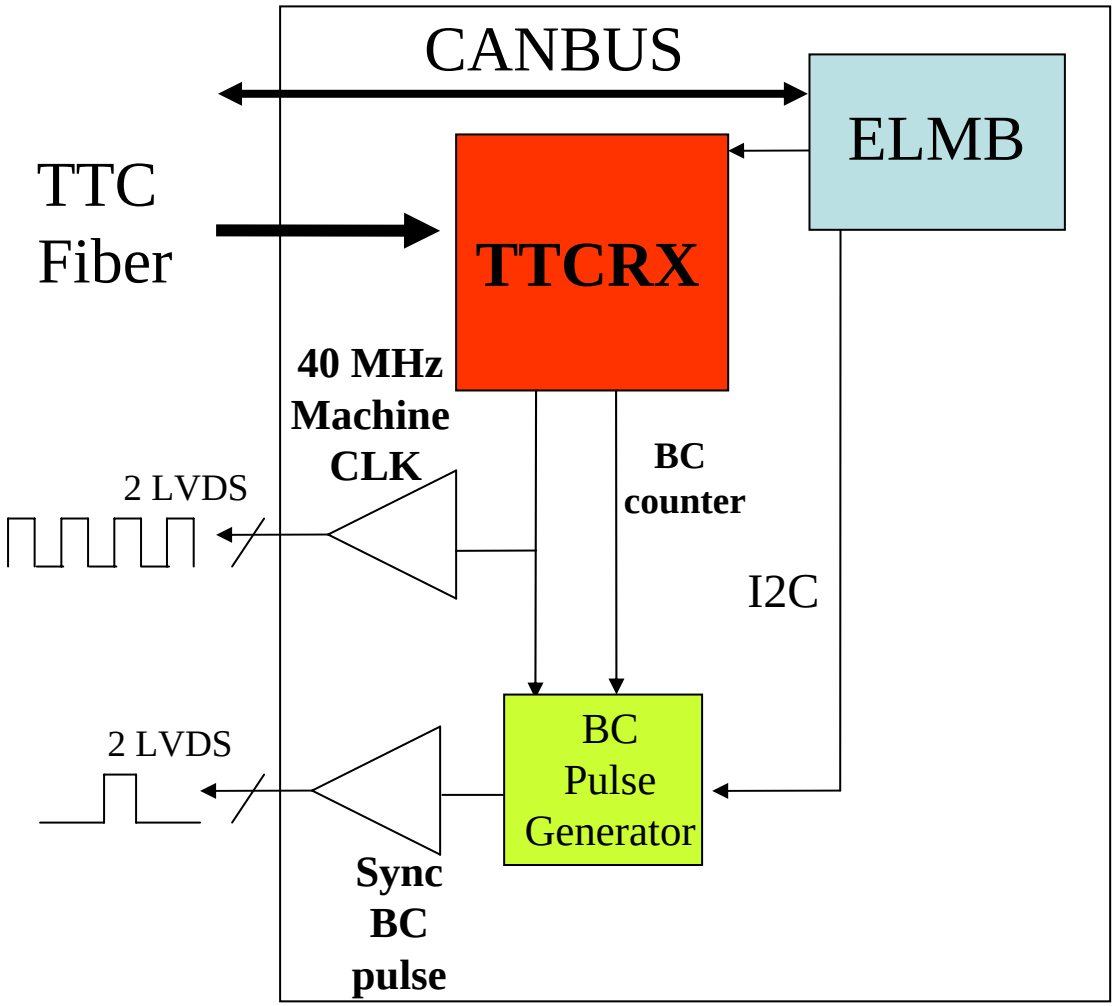
PCI Board
Kvaser CAN

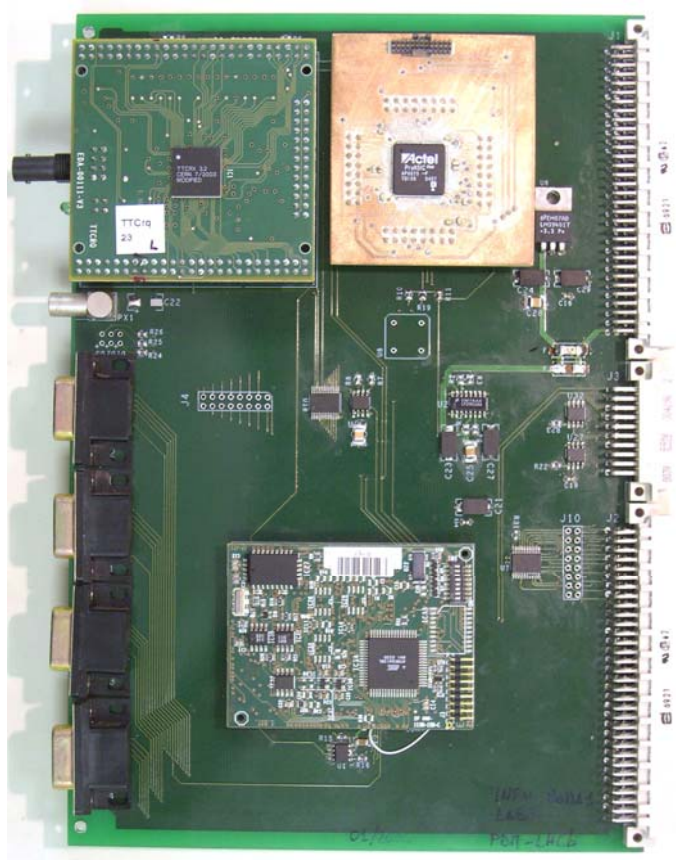
4x256kbps



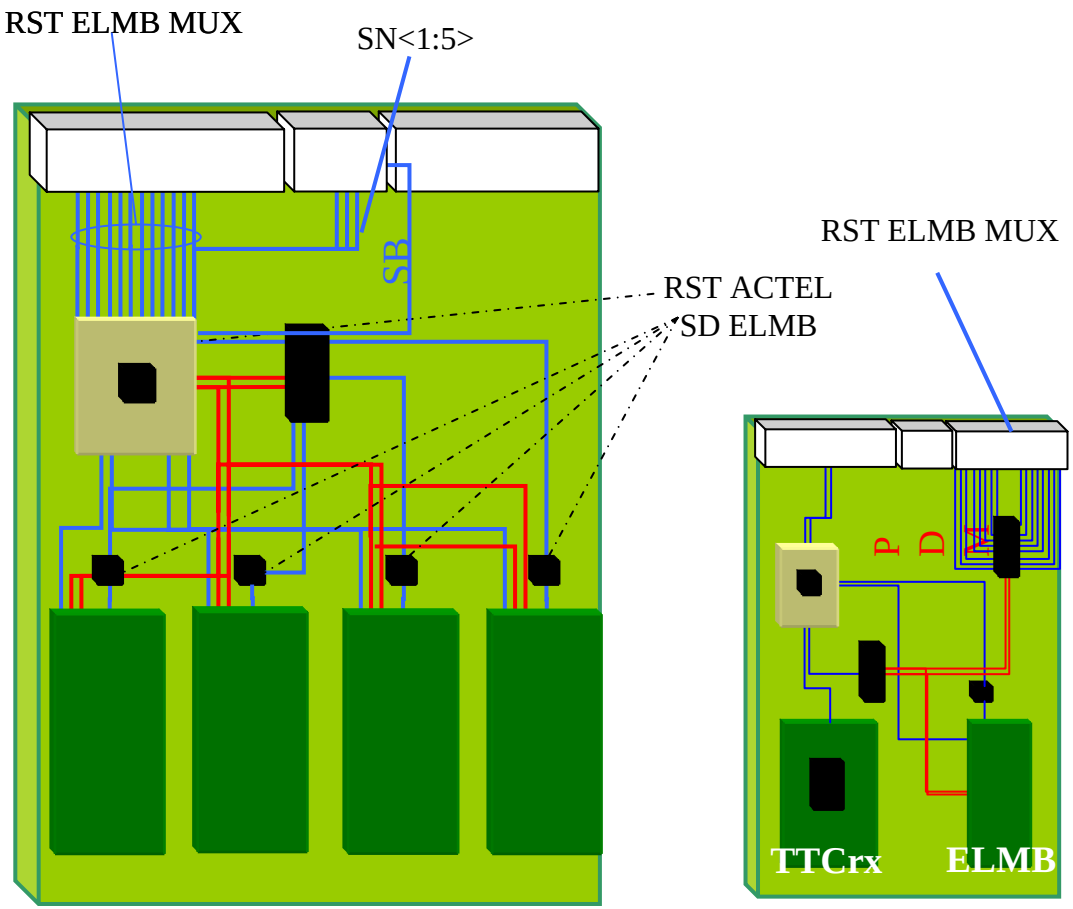


Pulse Distribution Module

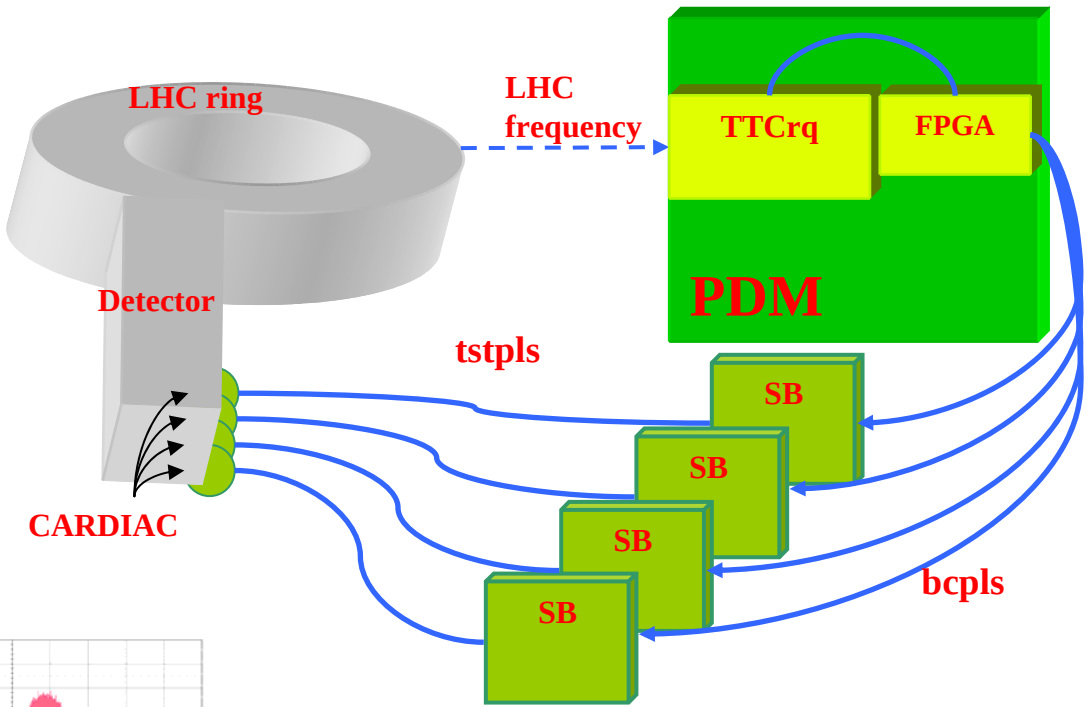


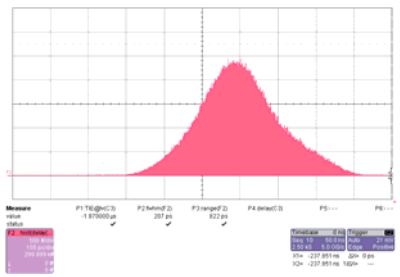


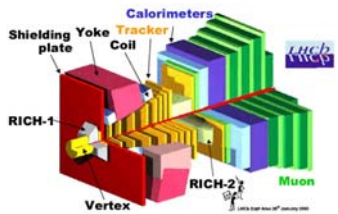
Shut down and Reset *SB and PDM*



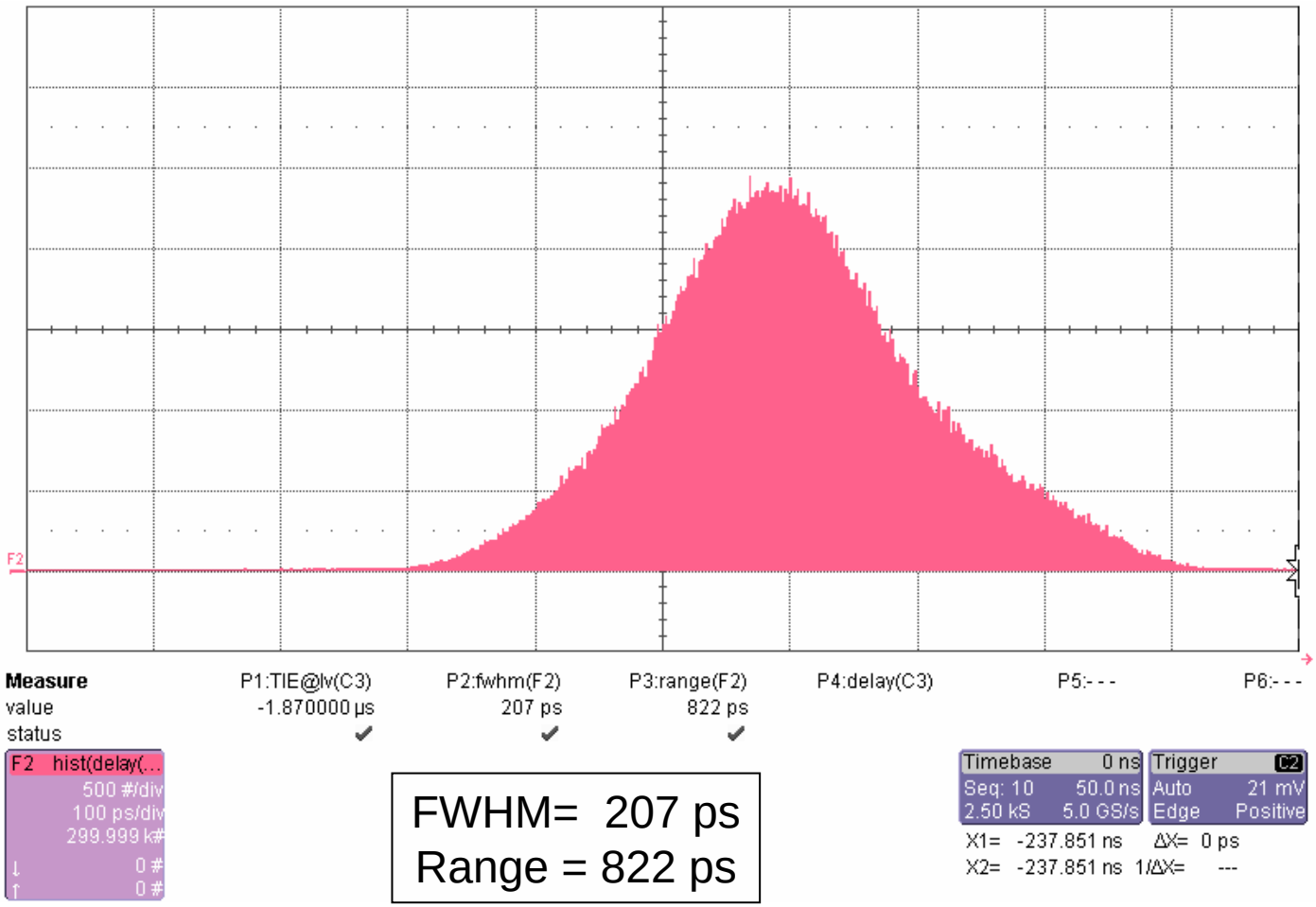
PDM Pulse path





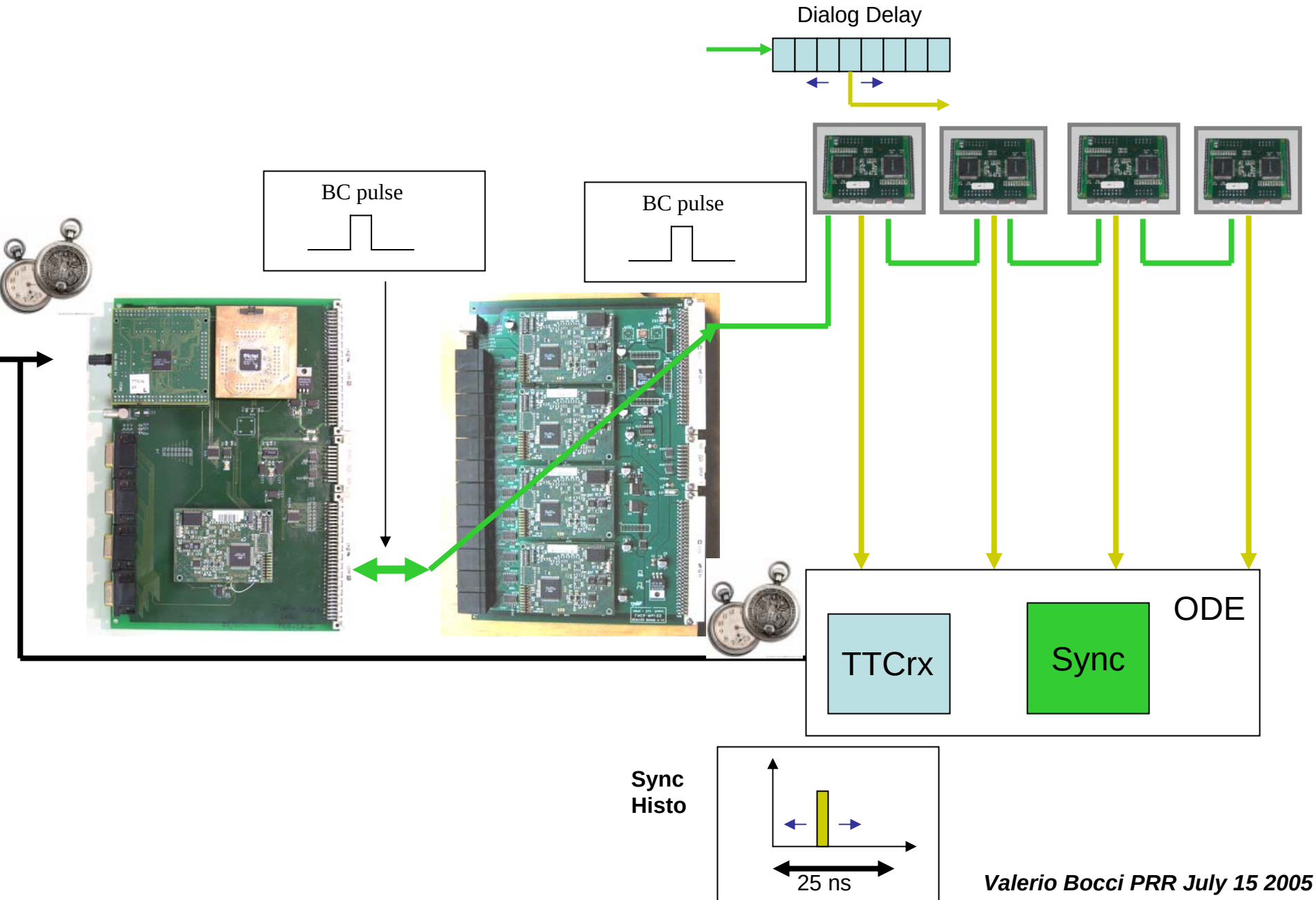


TTCvi->TTCRx>PDM->SB->I2CLVDS Jitter



FWHM= 207 ps
Range = 822 ps

Fast coarse Time Alignment (Without physics)



Conclusions

- Service Board prototype was useful tool for chamber test
- The FPGA flash was a big advantage
- We have 10 preproduction board under test

- PDM prototype is working fine we want to finalize the design with new feature.
- We decide to design a custum backplane instead of a customized vme430 (cost reason)