Front end boards

W.Bonivento, S.Furcas and D.Marras (Cagliari)
+ V.Bocci,R.Nobrega (Rome I)+G.Auriemma and M.Martino(PZ)

1) quick review of status and organisation
2) board description
3) lab tests
4) chamber tests

The LHCb muon electronics project

Common project with wire chambers:

1) same far-end structure
2) same front-end board conception: 2 CARIOCA chips + 1 DIALOG chip
3) same bids and producing companies
4) same people

BUT

1) CARIOCA → CARIOCA GEM
2) front end board (CARDIAC) of different size and layout
3) SPB integrated on the CARDIAC
4) different cables and connectors

} space requirememnts

Status

- contracts for production signed
- 200 pre-production boards for WPC received:

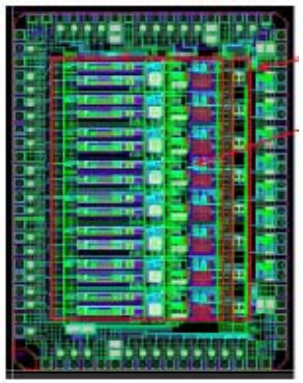
→150 tested: 50 in Roma1 (setup which will become CARDICACGEM prduction test setup) and 100 in PZ (setup which will become CARDIAC production test setup)

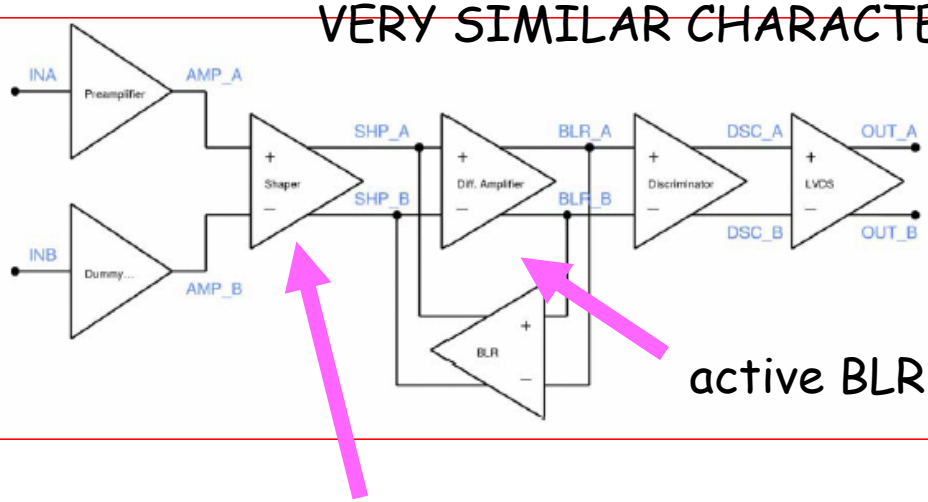
- 3 chamber types equipped for testing→OK
- ready to place the final order for CARDIAC after few WPC tests
- CARDIAC boards will be tested at the company site with PZ equipment
- rather tight schedule; company under purchasing of components
- expected production rate:2000/month (from Sepetember…)→total 9600

- 2 pre-production boards CARDIACGEM received; 54 expected by August
- production in October…→<400 boards →easy…(schedule less tight)
- CARDIACGEM boards will be tested at ROMA1

CARIOCA

VERY SIMILAR CHARACTERISTICS TO ASDQ





All differential circuitry, unipolar shaping →DC coupled

(CERN + CBPF Rio)

IBM 0.25 µm radiation tolerant technology
8 analog input channels
8 LVDS output channels

shaper, 2pole-zero ion tail cancellation

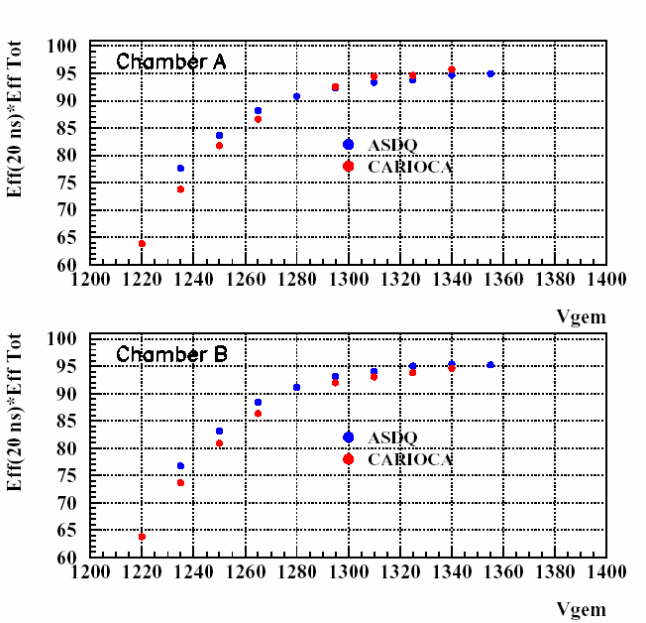
Discriminator threshold can be individually set to compensate for offset from process variation

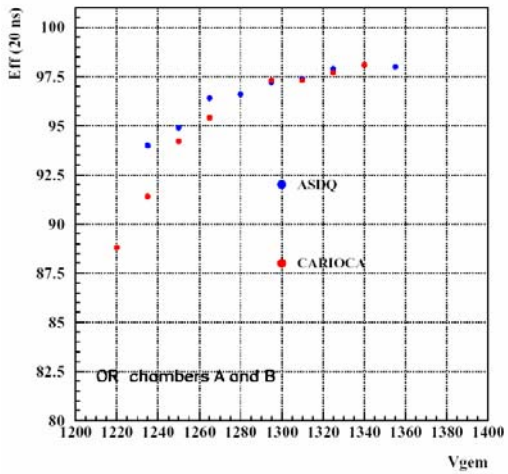
internal test structure to inject signal from DIALOG to CARIOCA input; minimum injected charge 50fC →only checks if channel ON/OFF

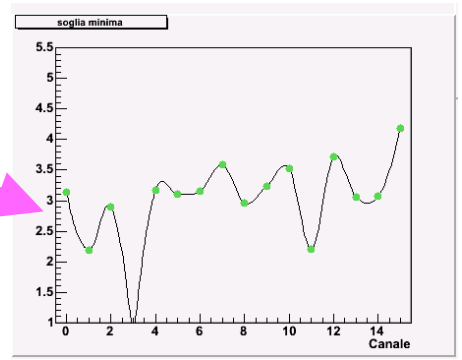
Why CARIOCA GEM and how

Two main reasons:

1)minimum threhsold: in beam tests with ASDQ it was set to 2fC; with CARIOCA10 the minimum is ~3fC



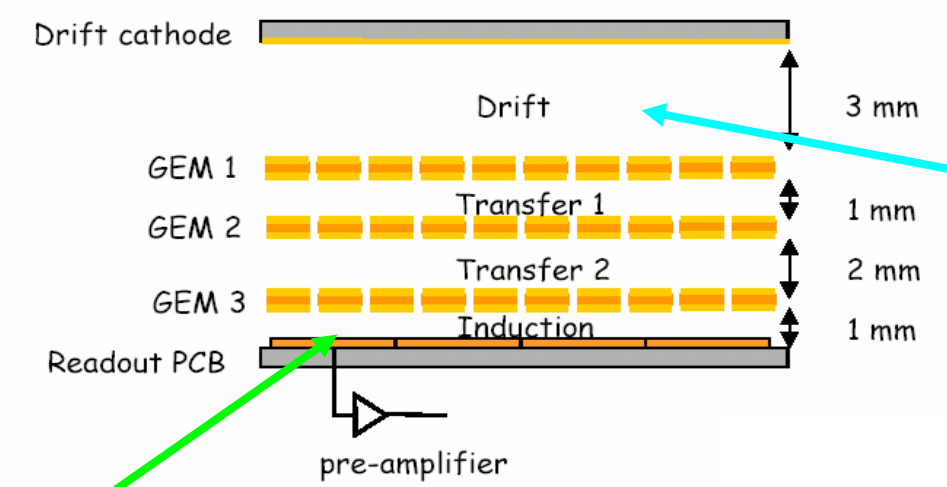




→10-15 V loss in plateau with CARIOCA

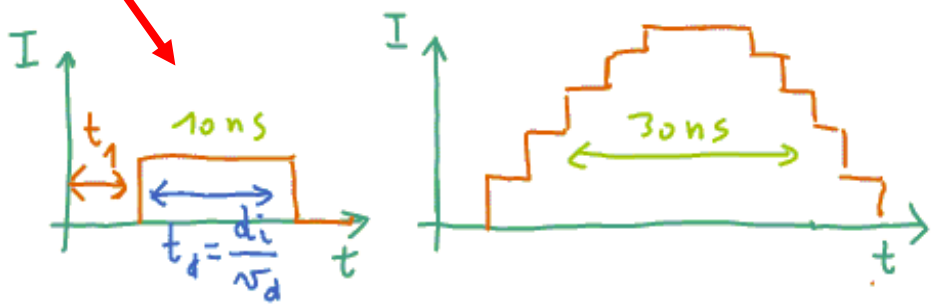
2) due to ion tail cancellation in the CARIOCA shaping circuit
→afterpulses

The triple-GEM detector signal



Primary ionisation and drift

Signal formation: same as pulse mode ionisation chamber



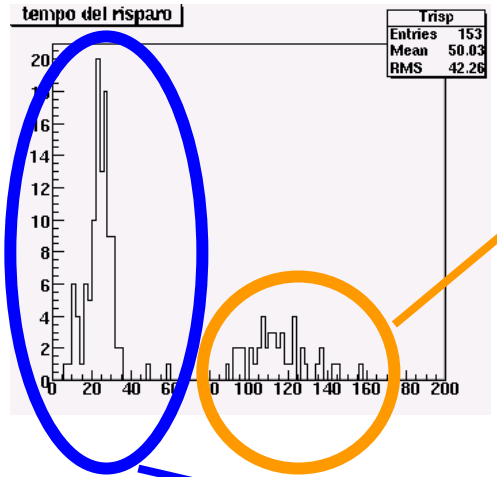
1 ionisation cluster

5 ionisation clusters

Example: 5 primary cluster signal

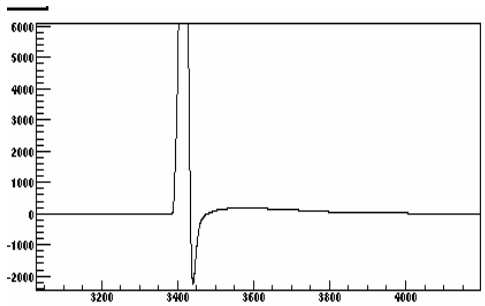
Afterpulses with ion tail cancellation

two reasons:

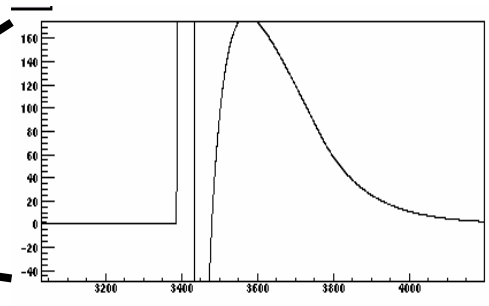


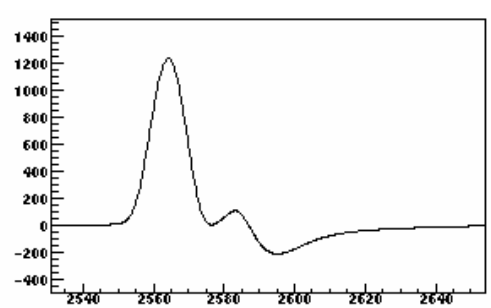
simulation

1) undershoot

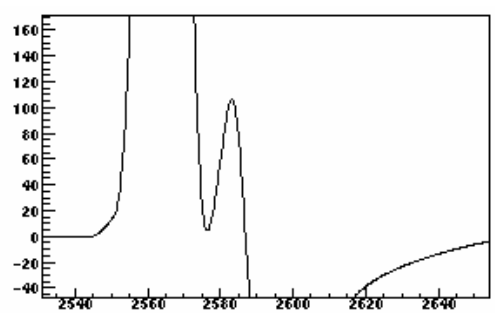


blow up





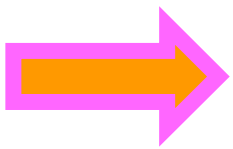
blow up



2) inside the event: different gain of clusters

irreducible fraction of afterpulses→ 10%-15%

Why CARIOCA GEM

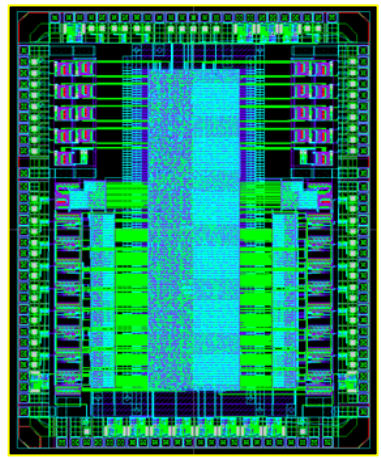


get rid of tail cancellation + increase the gain

To minimise the impact of the larger pulse width on the dead time →gain *1.5

DIALOG

IBM 0.25 μm radiation tolerant technology
16 LVDS input channels
8 LVDS output channels



INFN -CA

- **generates logical channels by OR-ing of two face-to-face physical channels**
- provides a masking facility to access single channels
- **threshold DAC and line drivers for the CARIOCA chip**
- integrates 16 8-bit DACs with output buffer to set the CARIOCA discriminator threshold with about 0.17fC granularity
- **Programmable delays** → 31 steps of 1.6ns →50ns max
- **Digital shaping** →output signal width 8 steps of 3ns →25ns max
- **Front-end rate and noise monitor** 16 24-bits rate counters
- all functionalities can be controlled via **I_2C interface**
- Triple-voted and auto-corrected register for better SEU immunity

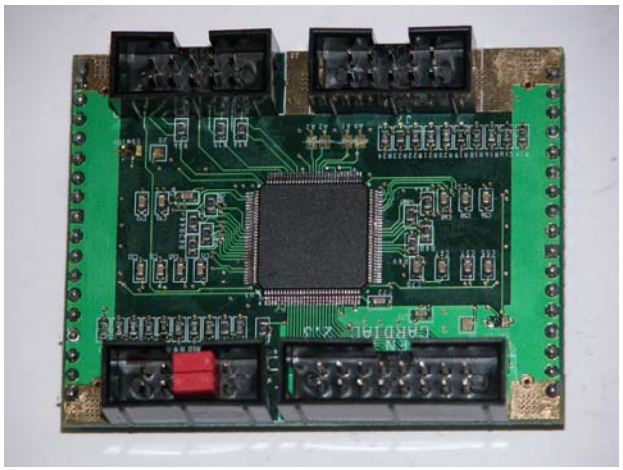
Front-end board structure

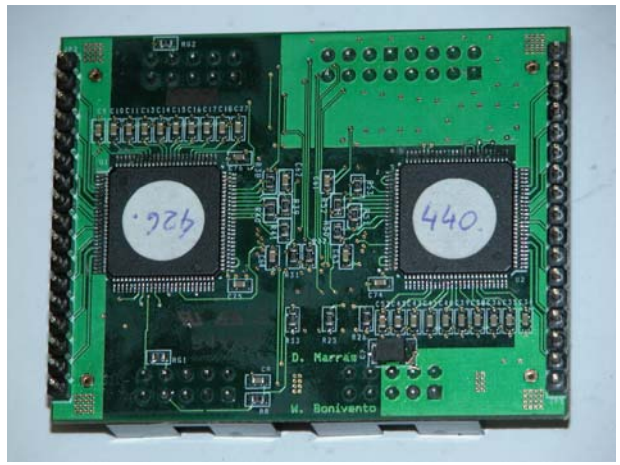
- 6 Layer, 1.6mm thickness, gold plated printed circuit board
- Two identical ground planes
- One power plane
- Three connection layers. Top layer mainly dedicated to LVDS digital signals, bottom layer to analog input signals and inner layer to I2C and other control lines.
- CardiacGEM board includes spark protection circuitry.

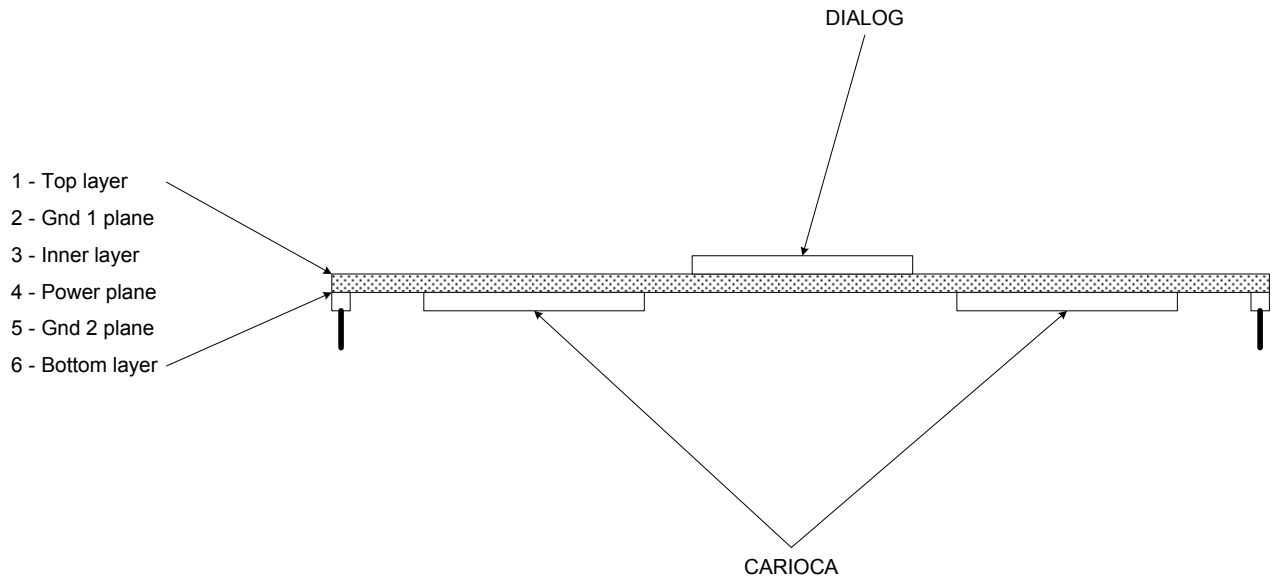
Ground issue

- The design inherited by Cagliari group was a 4 layer PCB, but with separate ground and power planes for analog and digital connection; equipped with two ASDQ chips.
- Many prototypes have been made to test other grounding solution and to migrate from ASDQ to CARIOCA chip (CARIOCA7, CARIOCA8, CARIOCA9 and CARIOCA10 versions).
- Final design has been chosen because proved to be the solution which gave less noise and more stability.

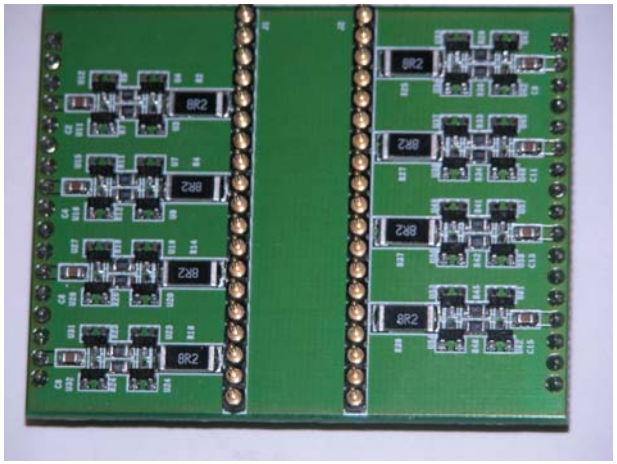
CARDIAC design

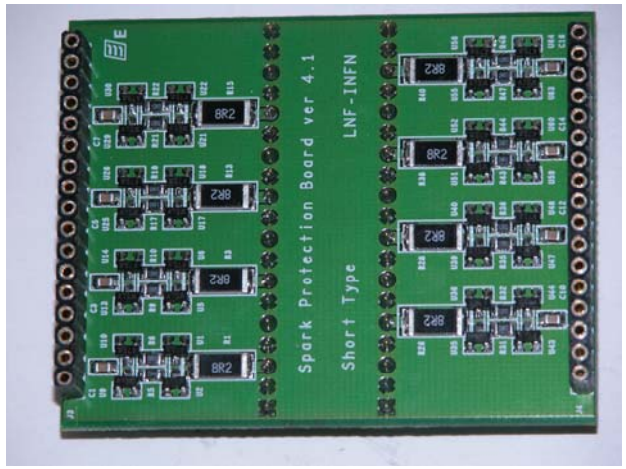


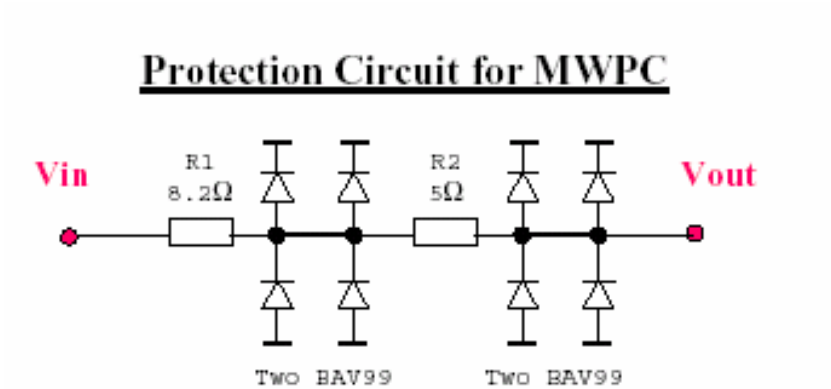




SPB design

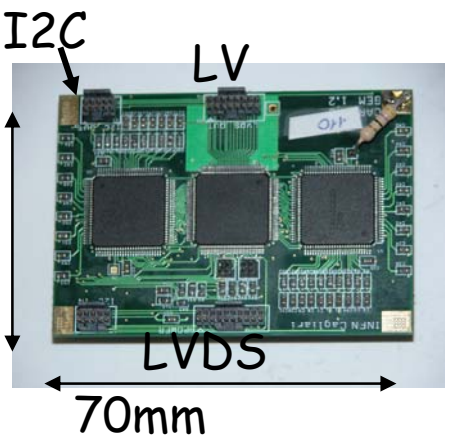



Spark Protection Board ver 4.1
LNF-INFN
Short Type

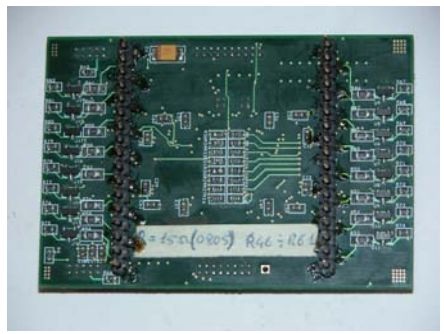

Protection Circuit for MWPC
Vin
R1
8.2Ω
R2
5Ω
Vout
Two BAV99
Two BAV99

The front end board for GEMs: CARDIAC GEM

- CARDIACGEM → 2 boards under test
- Tight space requirements → 45x70mm length and 14mm thichkness
- Two boards in one: FEB+SPB
- Spark protection on the bottom; the 3 chips on the top
- New type of connectors and cables →pitch reduced by half
- Need a special cable 0.5" pitch

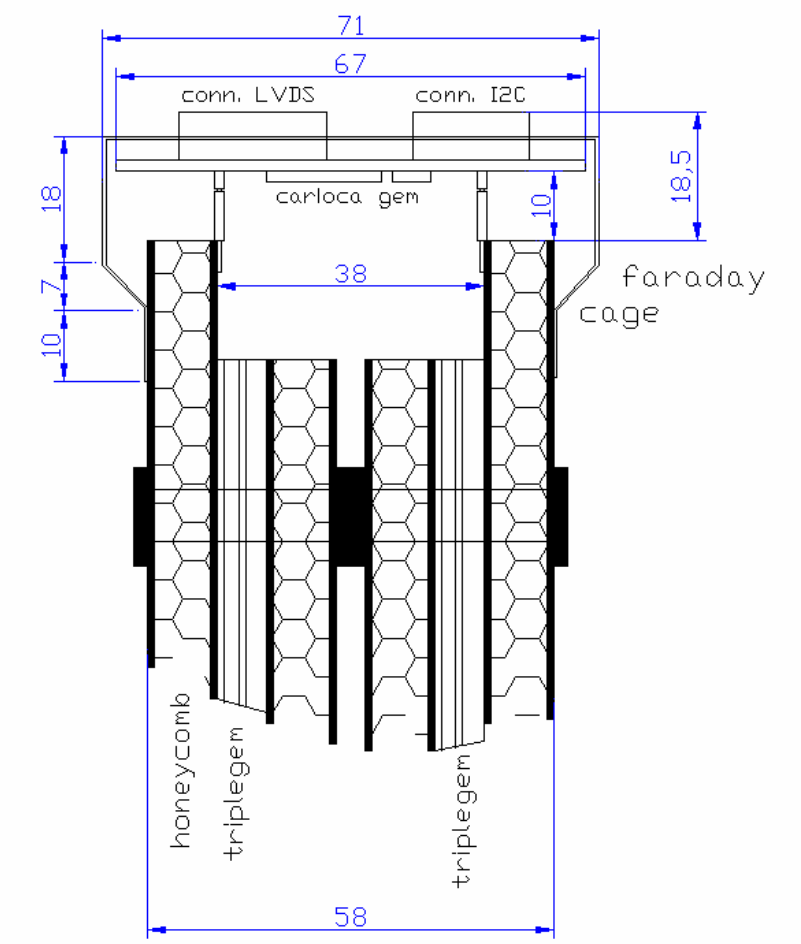


top



bottom

How the board is plugged in



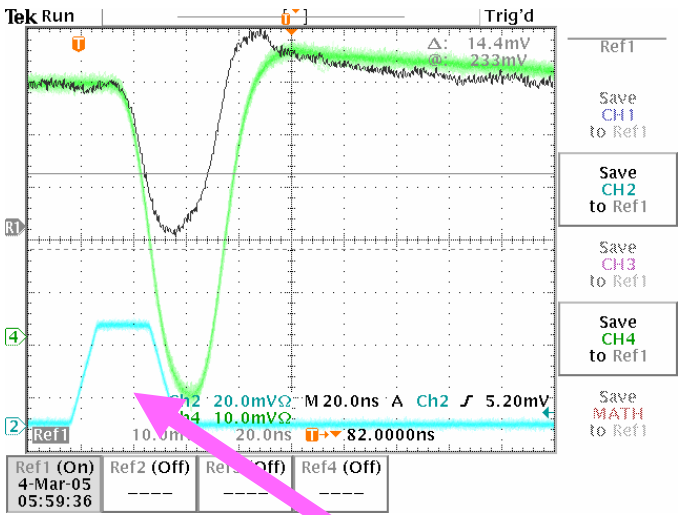
Minimum space available on the top for cables 5-6mm

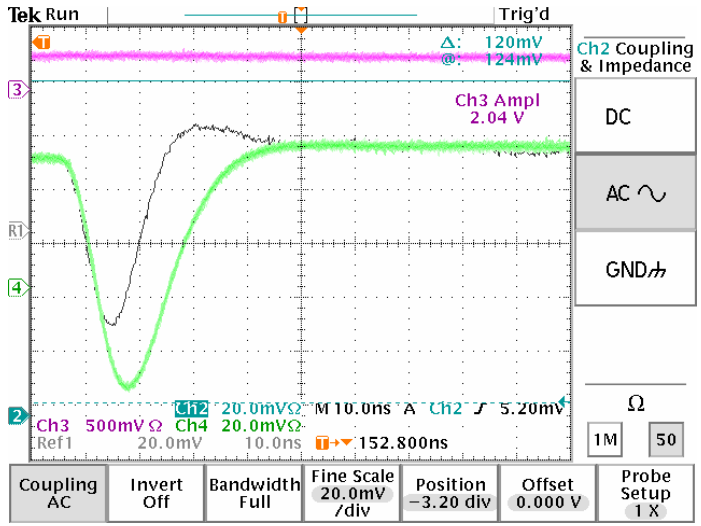
Test bench measurements

Analog shapes

CARIOCA vs CARIOCAGEM

Cdet=15pF

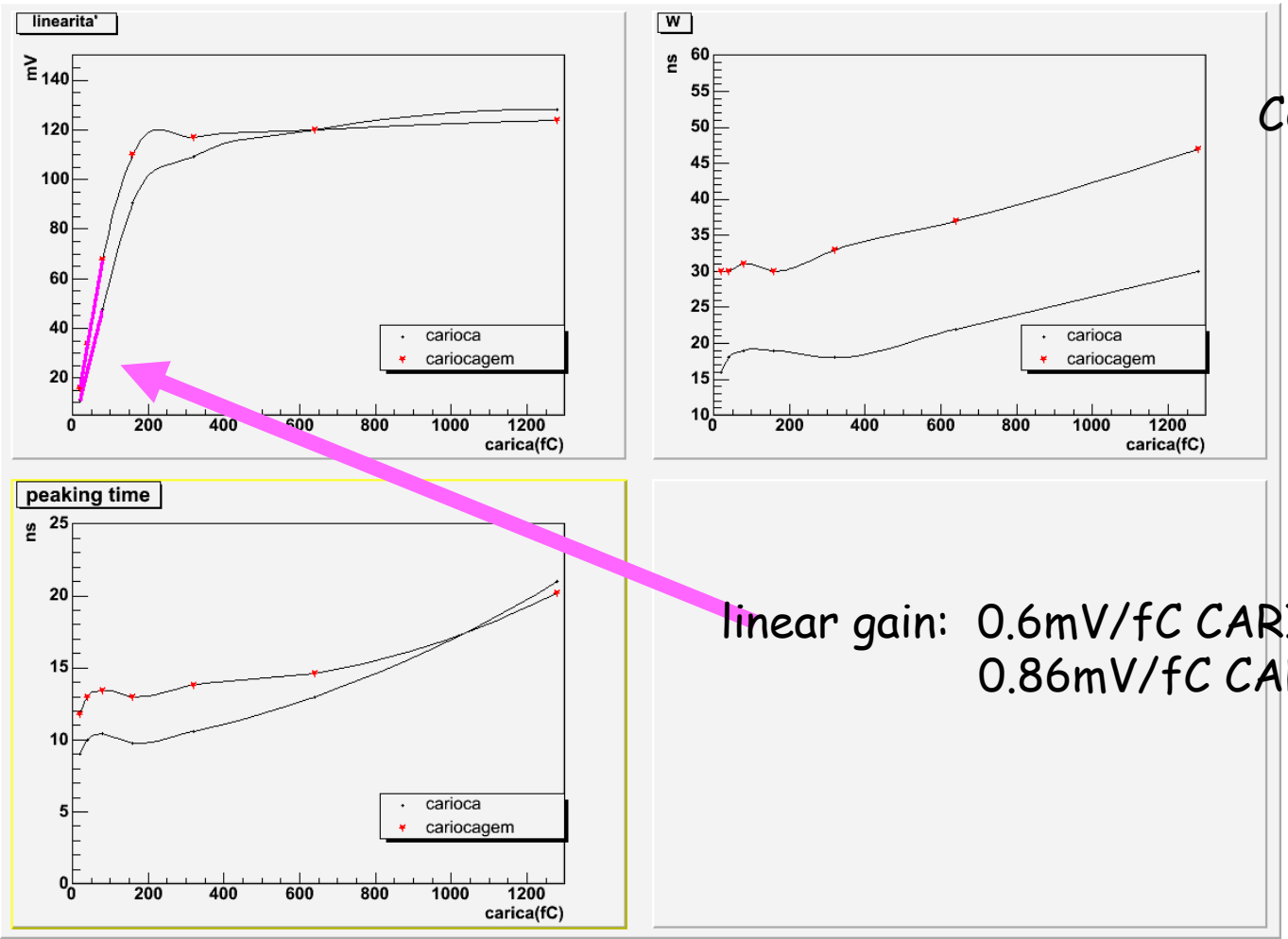




delta response
~1.5 of gain

response to GEM signal

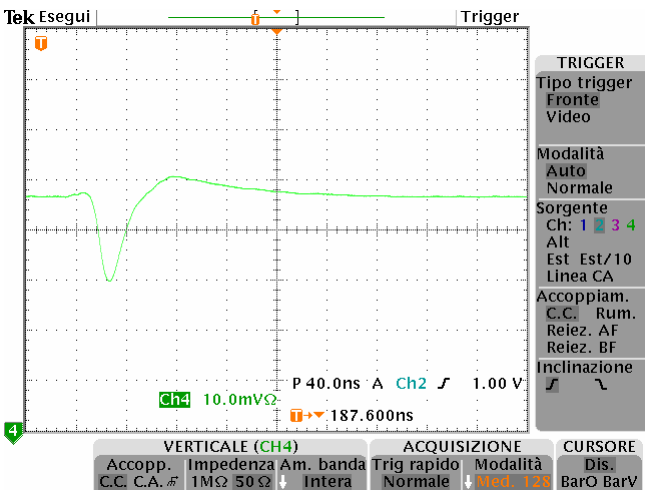
Analog response to δ

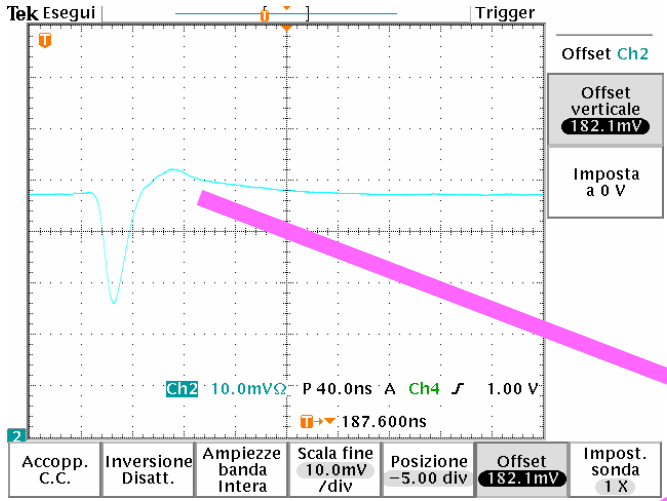


Cdet=15pF

linear gain: 0.6mV/fC CARIOCA
0.86mV/fC CARIOCAGEM

Analog shapes to δ

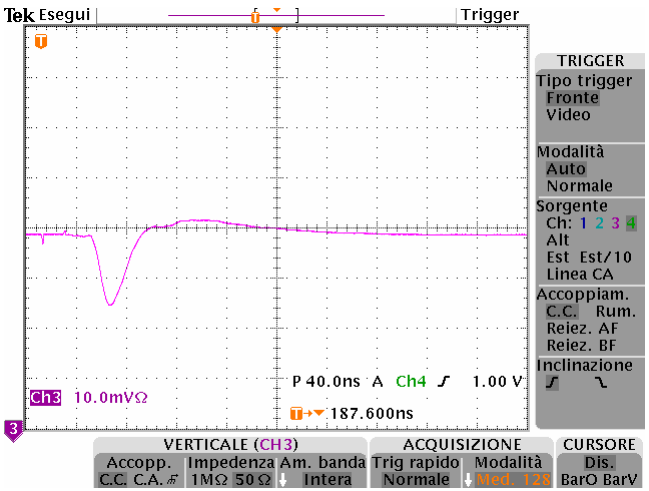


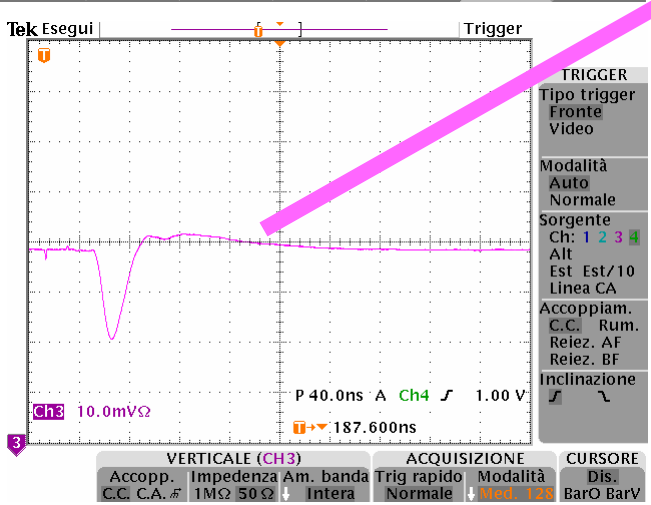


positive amp

No oscillation

negative amp

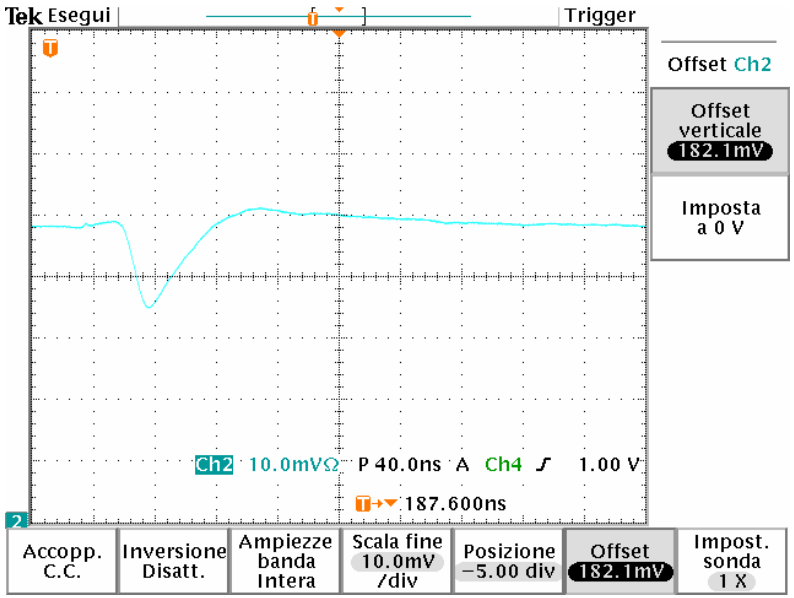




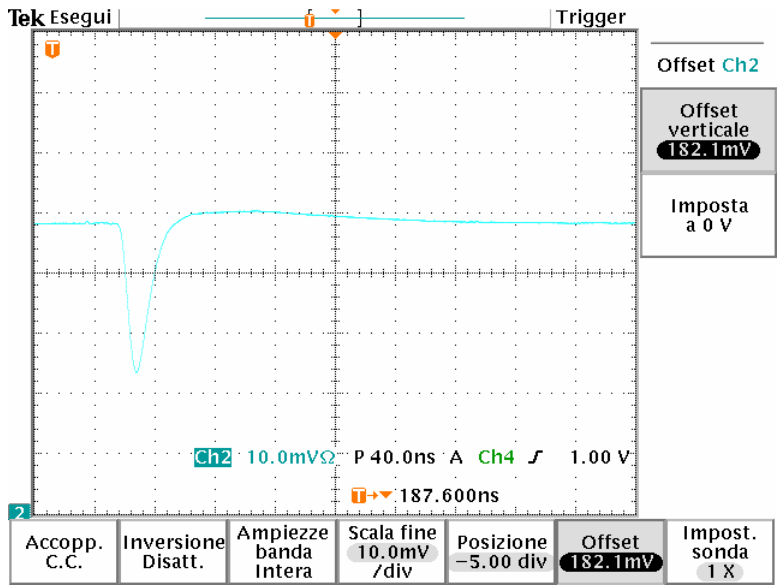
Cdet=220pF

Cdet=150pF

Analog shapes to 1/t



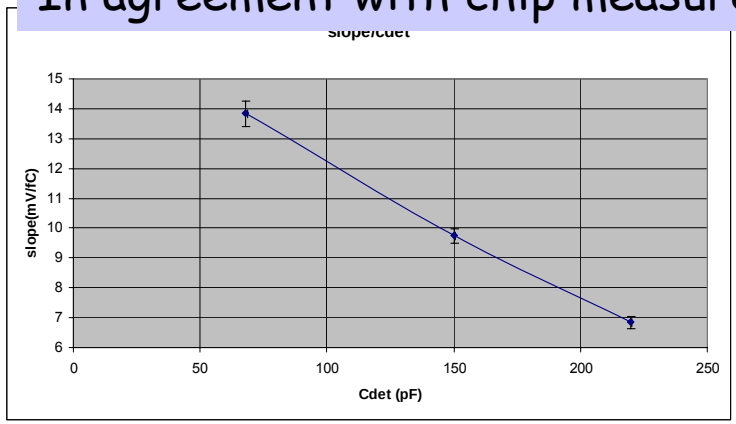
Cdet=220pF



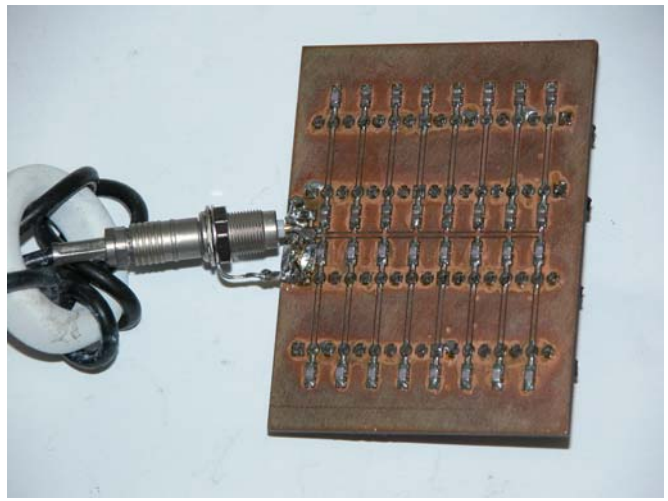
Cdet=5pF

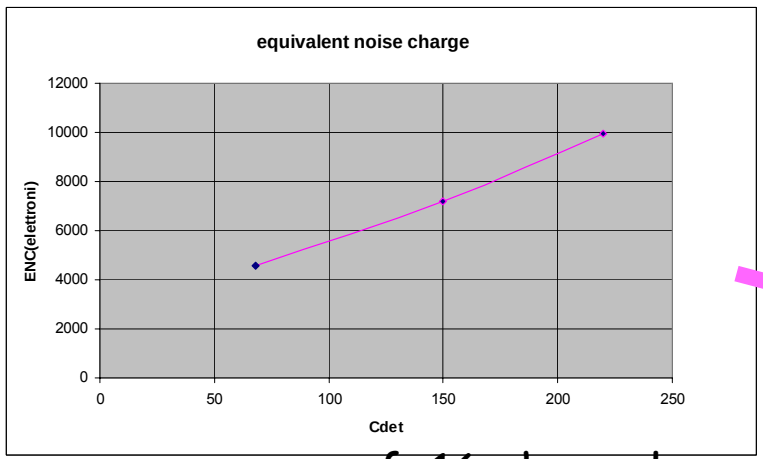
CARIOCA vs Cdet

In agreement with chip measurements in RIO and CERN mesurements



negative amp

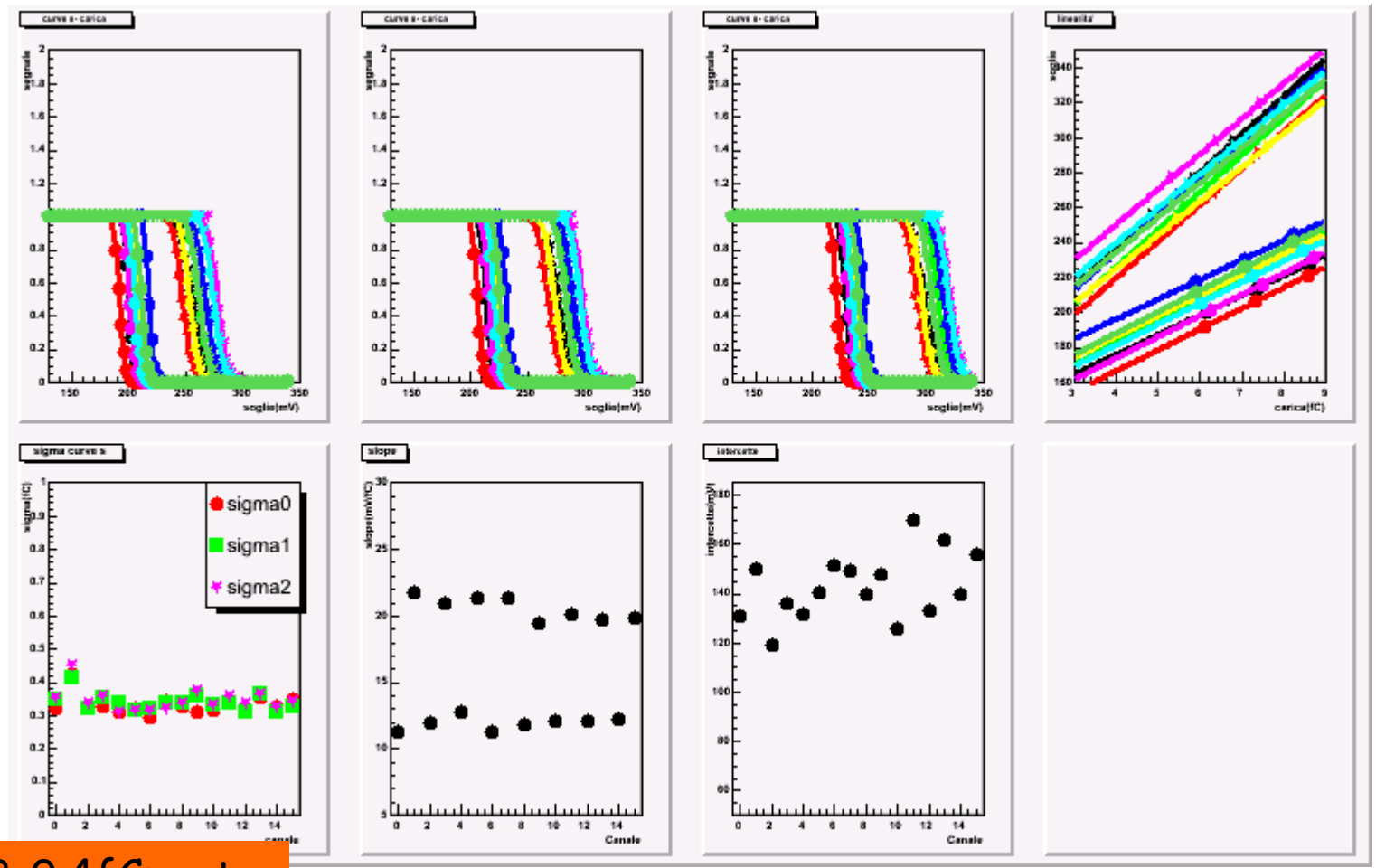




average of 16 channels

Noise<2fC at the highest Cdet→OK

CARIOCA vs CARIOCAGEM



ENC~0.3-0.4fC; not depending on channel position: other

Cross-talk

Always measured to be <0.5%

Also tested with parallel injection of all channels of one chip and looking at the other chip

And also all channels of the board but one→again <0.5%

Test of pre-production

Done with two test setup:

a) 100 boards in Potenza → CARDIAC production test bench (see Auriemma talk)

b) 50 boards in Rome1 → CARDIACGEM production tetst

Results as expected (noise and gain)

Yield: 80% (from tested chips)→to be improved…with the company

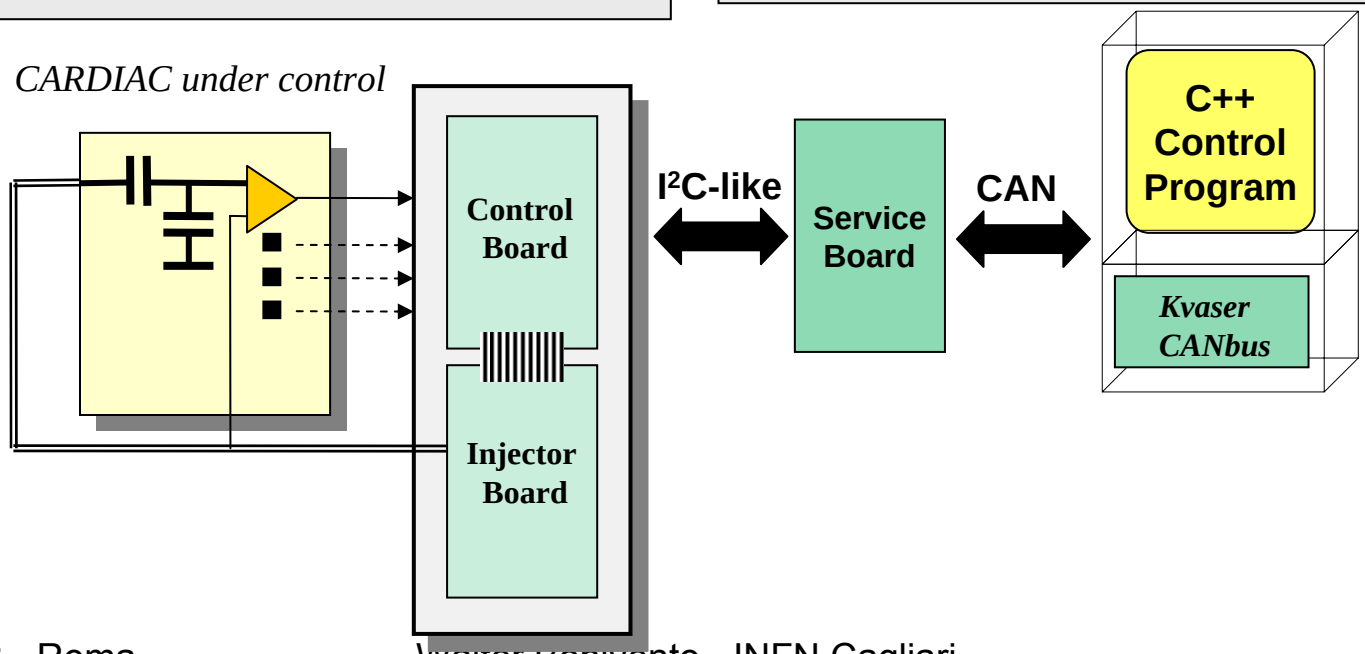
Overview of the Rome1 setup

Injection Board

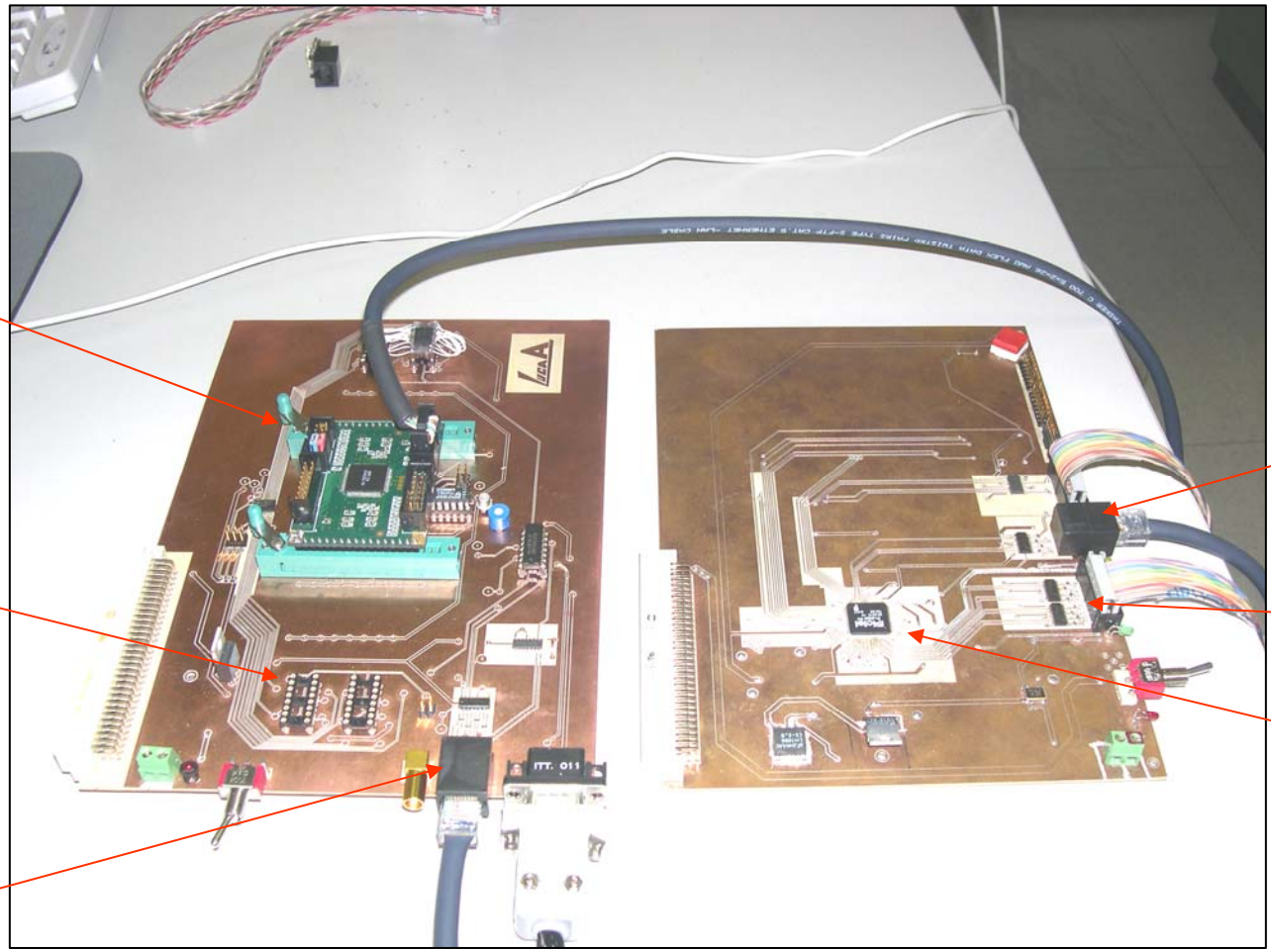
- 16 Injection channels
- Mask out injection lines
- Variable Injected charge
- DAC placed on Board
- Positive and Negative injection
- I²C and I²C-like compatible

Control Board

- Readout based on a FPGA
- 8 counters implemented
- 8 LVDS read-out channels
- I²C and I²C-like compatible
- USB Interface
- TDC

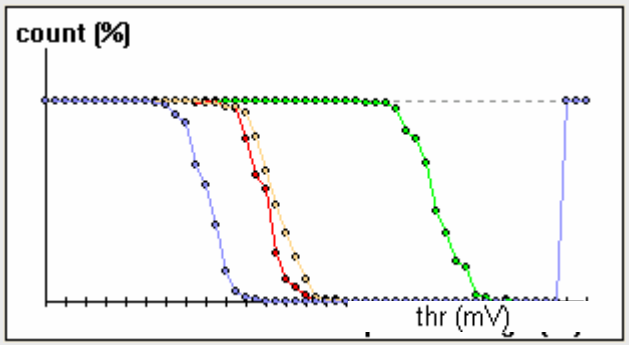


Picture of the Rome1 setup

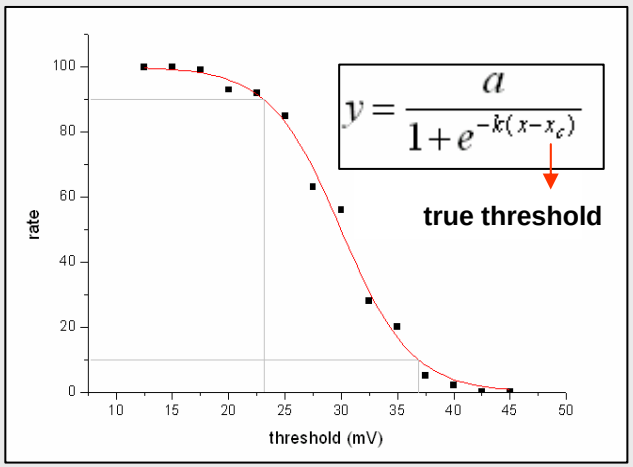


Software Measurements of Parameters

Noise (using threshold or charge scan)



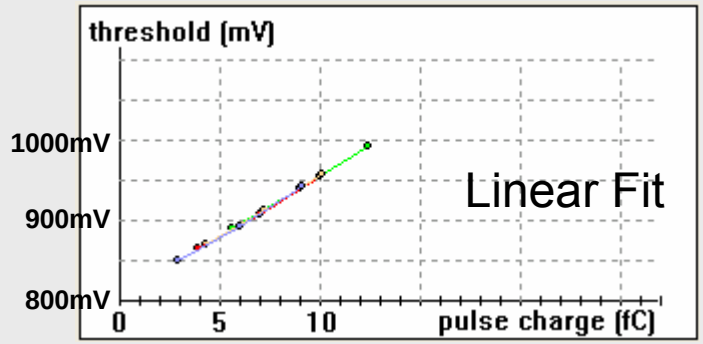
Non-Linear Fit (Levenberg-Marquardt)



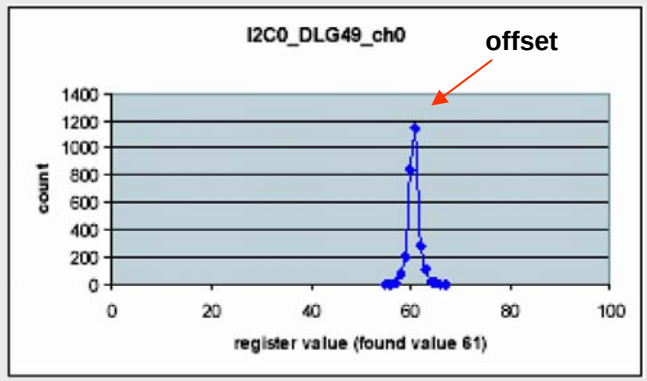
Noise rms (10% - 90%)

2.56

Sensitivity



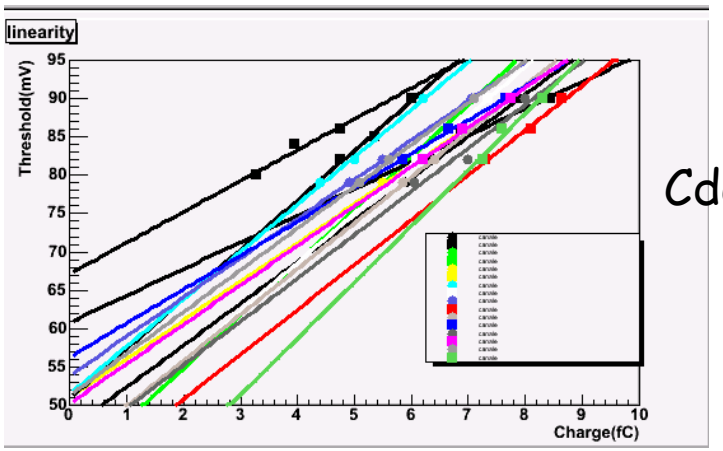
Offset (by curve extrapolation or noise measurament)



Threshold calibration(I)

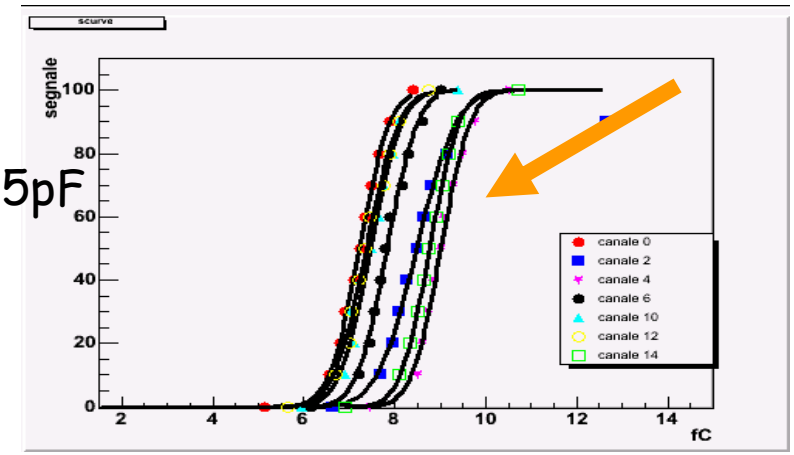
Standard lab tests (also at the Company assembling the boards)

gain curve

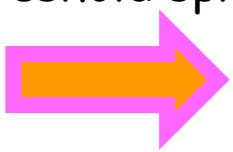


Cdet=15pF

S-curve



Problem: due to process variations →spread in gain curve parameters:
a)SLOPE b) INTERCEPT
If one threshold value for all channels is set, then about 1fC rms effective threshold spread is obtained

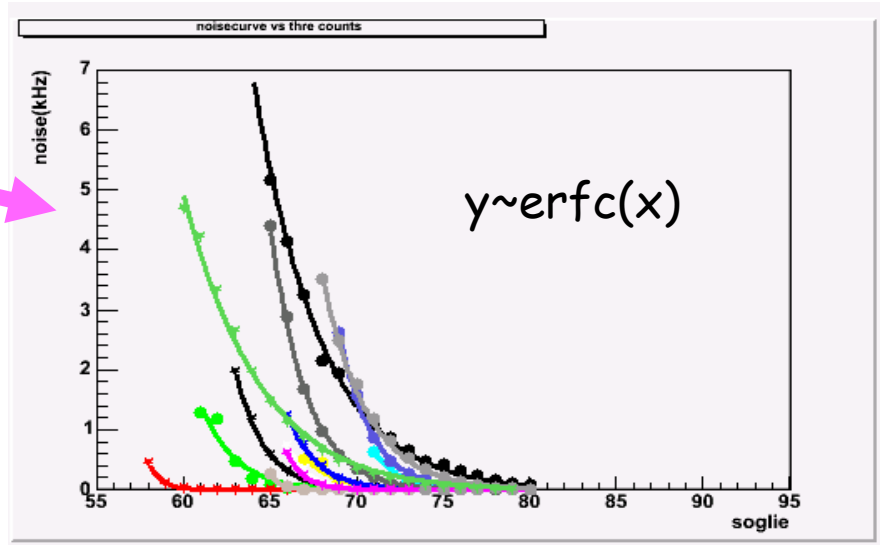


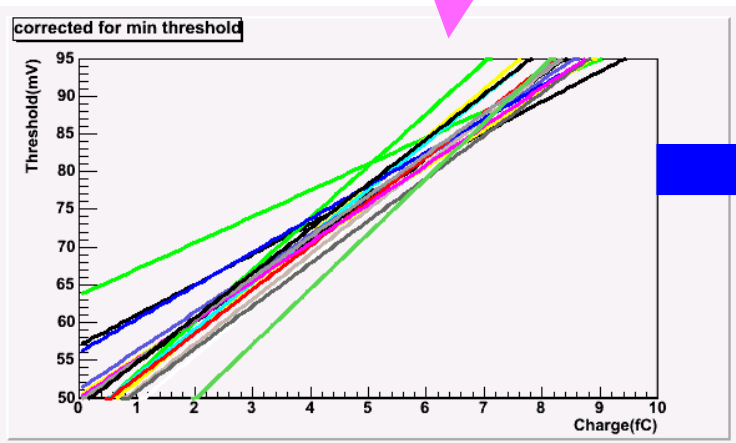
too much for GEMs (we want to trigger at ~2-2.5fC)
remember: WPC trigger at 6-8fC →much less of a problem…

Threshold calibration (II)

STRATEGY to reduce the threshold spread:

1) measure noise counts vs. TH curve
2) correct for the intercept spread equalising minimum thresholds (~1.5 fC in CARIOCAGEM)





effective threshold spread is reduced to about 0.5fC rms

This can be done in LHCb and continously monitored!

Threshold calibration (III)

A further improvement of the threshold spread (reducing it to ~0fC) can be obtained in the lab:

1) measuring directly the **gain** at the assembling company and keeping a database (foreseen in the contract)

$\Delta G/G(\%) = 0.5 \times \Delta T(^0C)$

$= 20 \times \Delta V(mV)$ of power supply

the same cannot be done for the intercepts since e.g.
$\Delta G/G(\%) = 1 \times \Delta V(mV)$ of power supply!!!
→20mV in supply voltage moves the intercept by 20% !!!!

→ the slope is much less sensistive than the intercept to supply voltage variations

→ we are lucky that the intercept spread can be compensated for with the other method…

2) injecting a calibration pulse on G3down

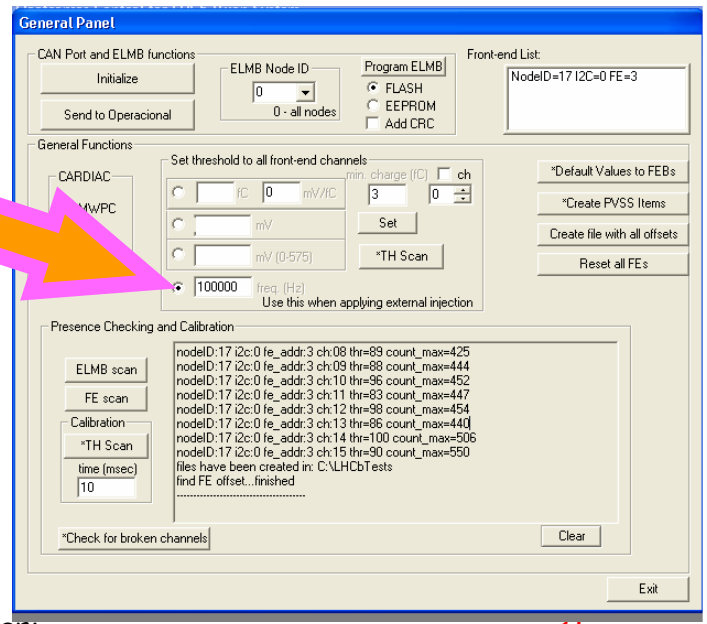
Threshold calibration on chamber for the GEM

A tool is available to set the thresholds automatically → injection from GEM3 down;

→ it allows to set the threshold with one CLICK automatically on all channels; the procedure is INDEPENDENT of the exact value of Cdet (between 15pF and 30pF in the final prototype).

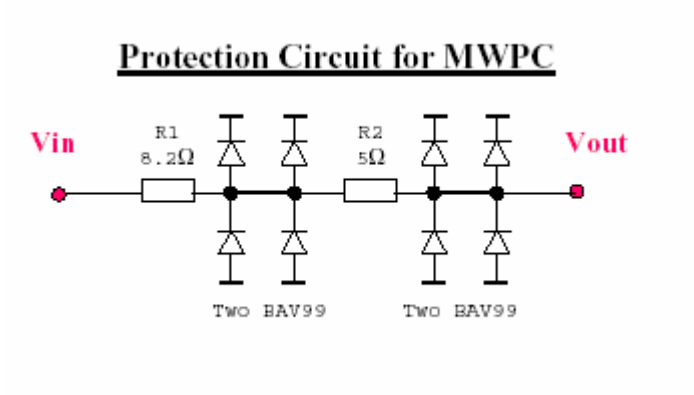
→ two possible ways

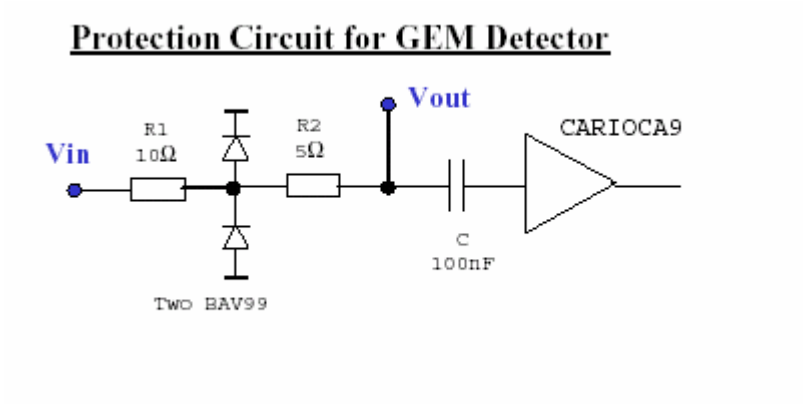
1) with the injection of a defined charge with S-curve
2) with fixed noise level

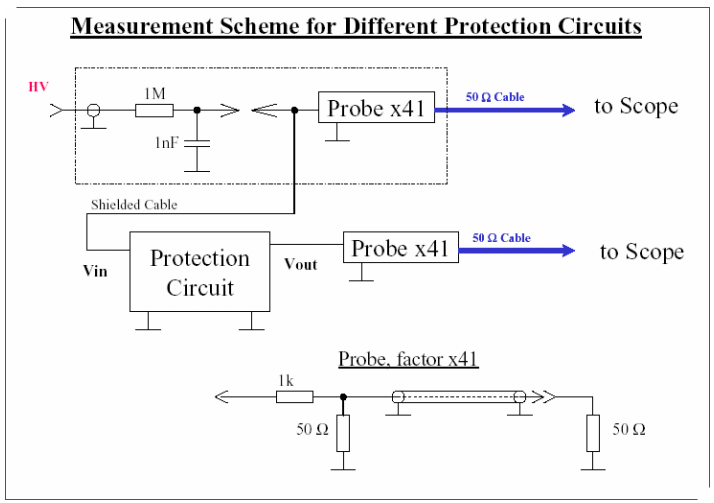


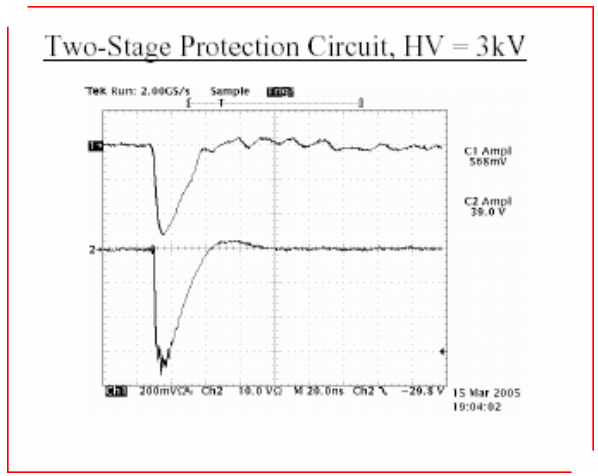
Rome I

Spark protection issues (Golyash)



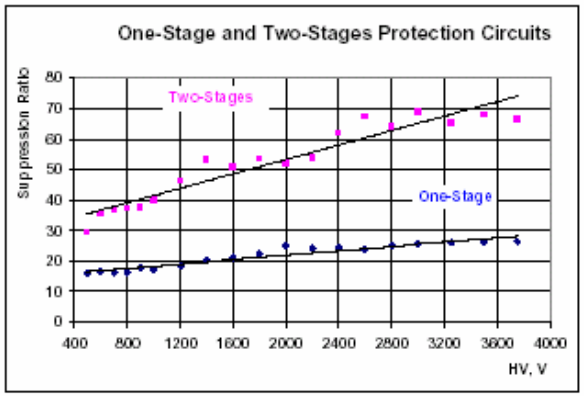


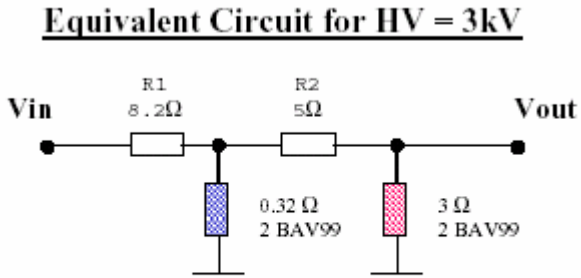


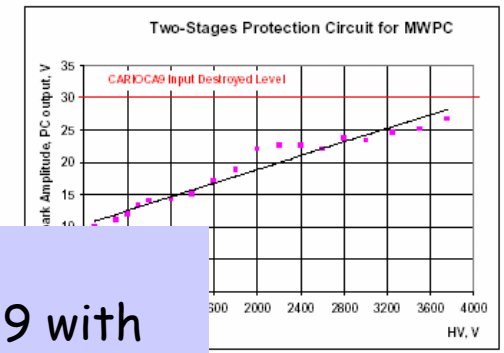


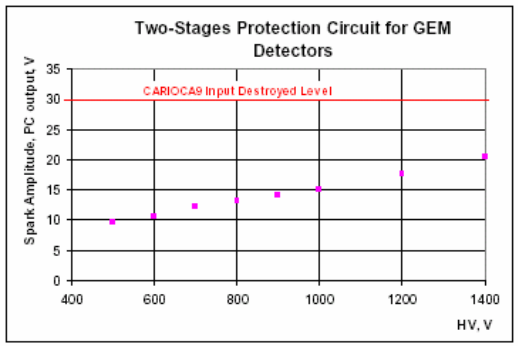
test performed witout L→conservative

Spark protection issues (Golyash)

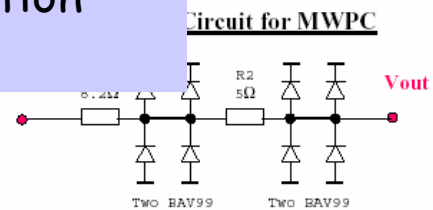


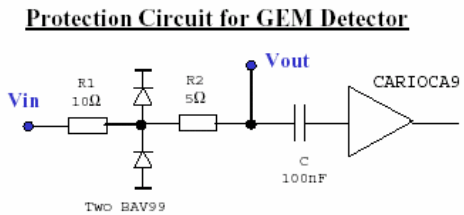






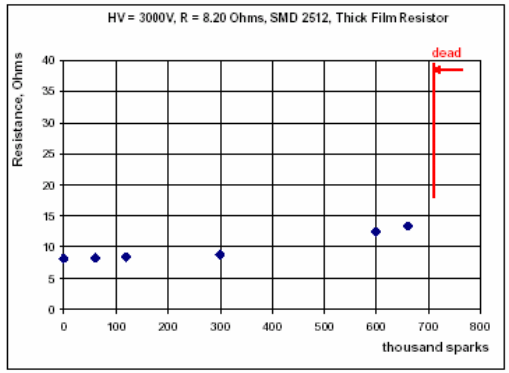
test of CARIOCA9 with the protection circuit



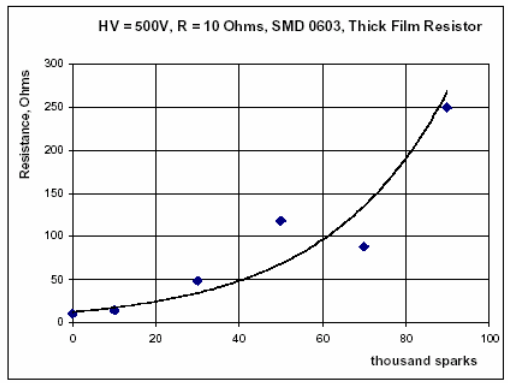


Spark protection issues (Golyash)

WPC



GEM



test of the first resistor

Chamber tests (MWPC)

In 2004 test were performed at GIF with the first prototype of the CARDIAC board:

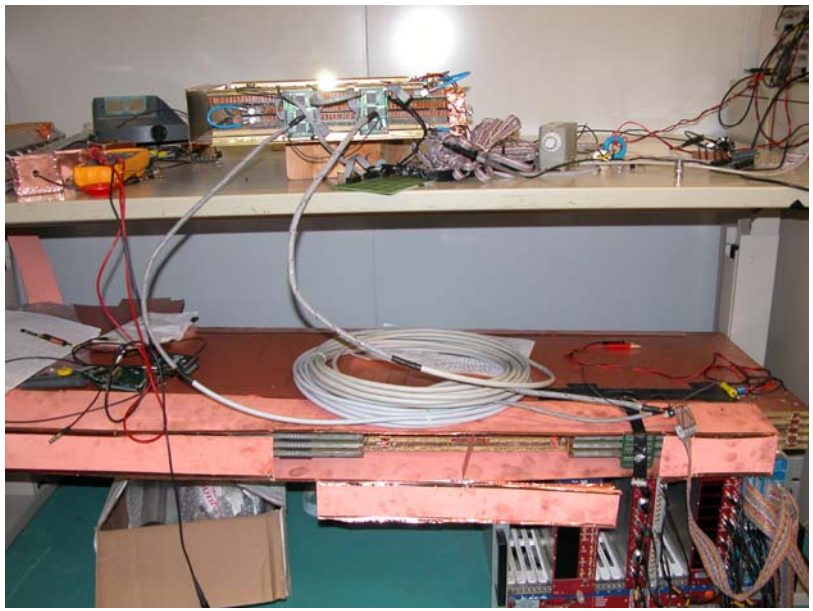
M3R3→pad Cdet=60pF
M3R1→pads

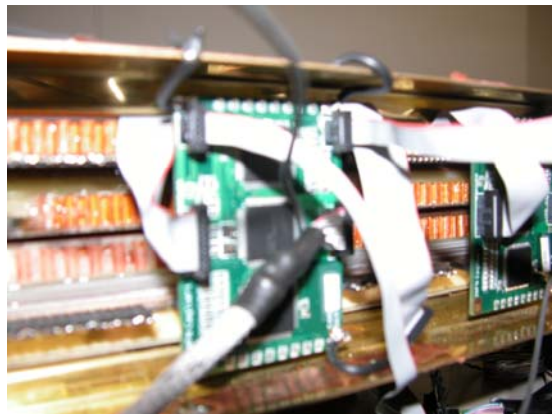
→ satisfactory results (see D.Pinci)

Now with last board version: tests at LNF with cosmics of(see D.Pinci)
M3R3→pad Cdet=60pF
M5R3→pad Cdet=150pF
M5R4→wires
Cdet=220pF
NOT SO EASY due to missing final FC, shielded cables etc →some problems could come from the chamber itself!!!

The CARIOCA10 chip was anyway also tested on:
M3R4→wires time resolution OK (only CARIOCA board)

Chamber tests (GEM)

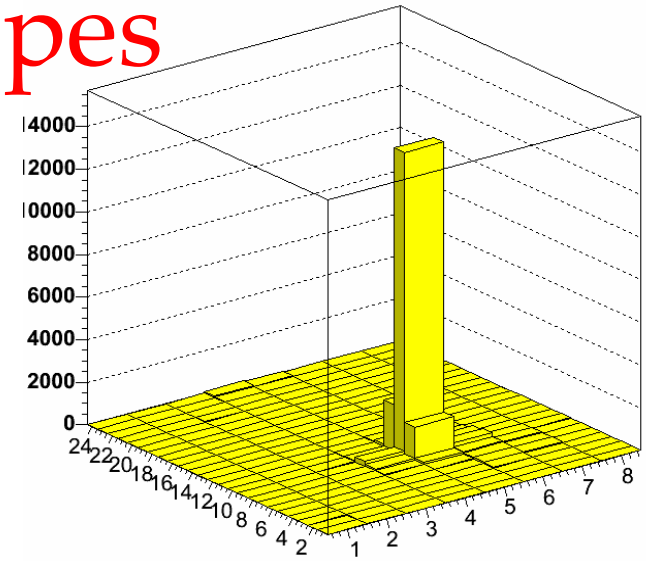


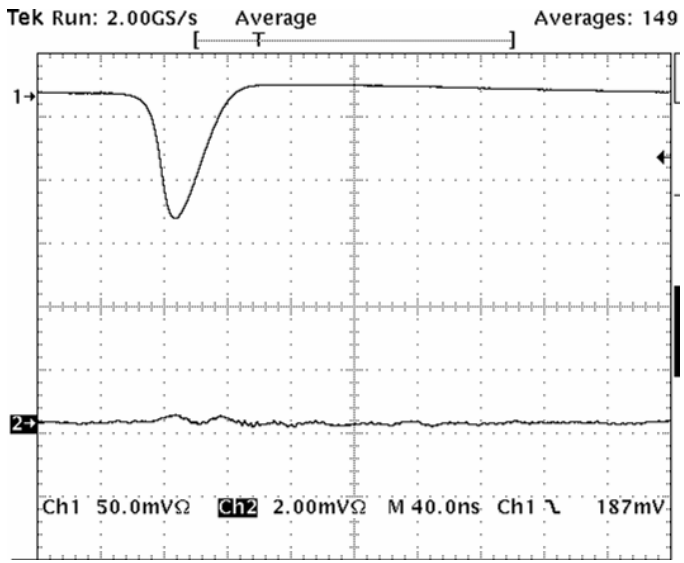


<1khz →2fC threshold
10m cables: special production
done at CERN: the last 10cm are 0.5" while the rest is 1"

Analog shapes

- ✓ ^{90}Sr 100 μCi
- ✓ Low energy electrons (~2 MeV)
- ✓ Collimator ➔ 0.5 mm ø
- ✓ Detector Gain = $2 \cdot 10^4$ (working point @ LHCb G=$6 \cdot 10^3$)





Conclusions

- WPC boards validated on three chamber types
- GEM boards validated on chamber (2 boards); need a full chamber test
- production issues, company and test stations, rather well set