ODE Board

Off Detector Electronics for the muon system

INFN - LNF
Servizio Elettronica Laboratori Frascati
A. Balla, M. Carletti, P. Ciambrone, G. Felici, M. Gatta

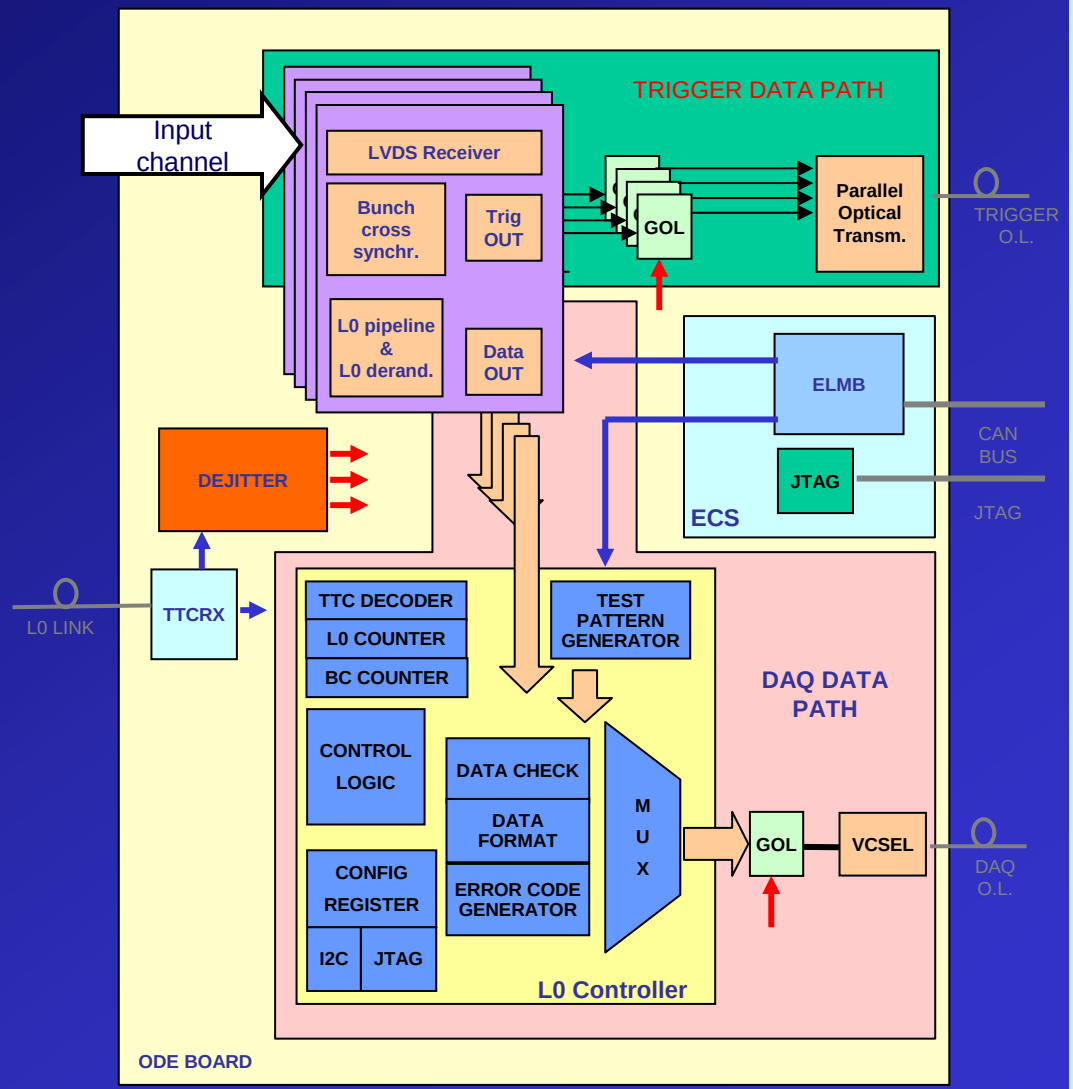
Outline

- ODE overview
  - Functionalities
  - Specs
- TTC system interface
  - Command and clock distribution
  - Measurements
- Trigger interface
  - Data flow and architecture
  - Performances
- DAQ Interface
  - Data flow and architecture
  - Performances
- ECS Interface
- GOL start-up problem
- Radiation hardness assurance
- System tests
- Conclusions

Paolo Ciambrone INFN- LNF

ODE overview

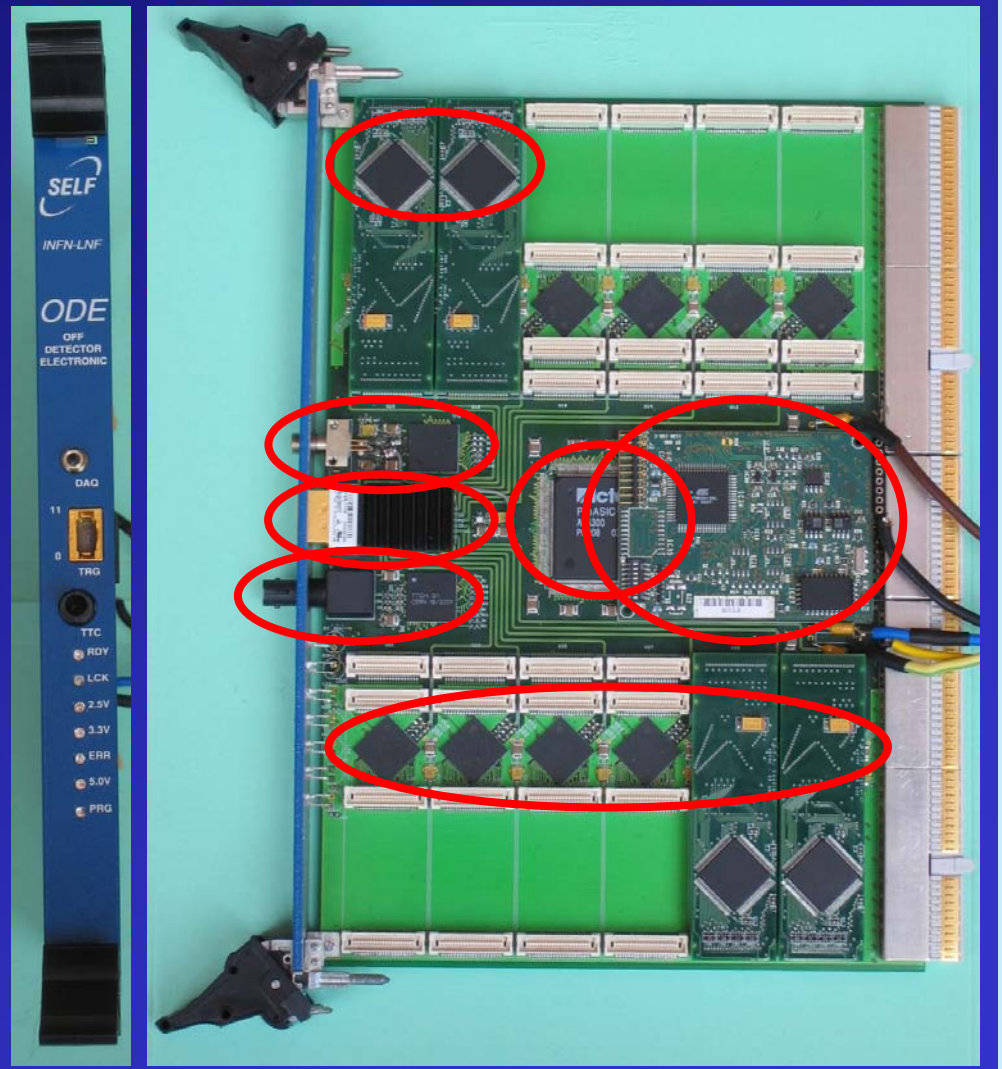
- L0 front-end electronics stage
  - Clock synchronization
  - Bx alignment
  - L0 pipelining and buffering
- TTC system interface
  - Master LHCb clock
  - L0 trigger and reset signals
- Clock de-jitter and distribution
- L0 trigger interface
  - Trigger Unit production
  - Parallel optical link
- L1 DAQ interface
  - Data formatting
  - Single optical link
- FPGA L0 board controller
  - TTC commands decoder
  - DAQ data formatting
  - Test facilities and diagnostic
- ECS interface
  - Initialization, monitor and debug
  - CANbus link



Paolo Ciambrone INFN- LNF

ODE specs

- L0 front-end electronics stage
  - 192 LVDS input signals
  - 24 SYNC chips (mounted on piggy board)
- TTC system interface
  - 1 optical receiver + 1 TTCrx chip
- Clock de-jitter and distribution
  - 1 QPLL chip
  - Tree network based on MC100LVEP family
- L0 trigger interface (12 traces @ 1.6Gbit/s)
  - 12 GOL chips + 1 parallel optical transmitter
- L1 DAQ interface (1 trace @ 1.6Gbit/s)
  - 1 GOL chip + 1 VCSel diode
- FPGA board controller
  - Flash RAM based Actel FPGA (ProAsicPlus)
  - 3 buses (32 bit) for SYNC and GOL interfaces
  - 154 I/O pin used (99%)
- ECS interface
  - 1 ELMB board
  - CANbus link on the backplane
  - 2 I^2C internal buses
- 6U Compact PCI card
  - 10 layers motherboard with controlled impedance
  - Mixed 5/3.3/2.5 V devices

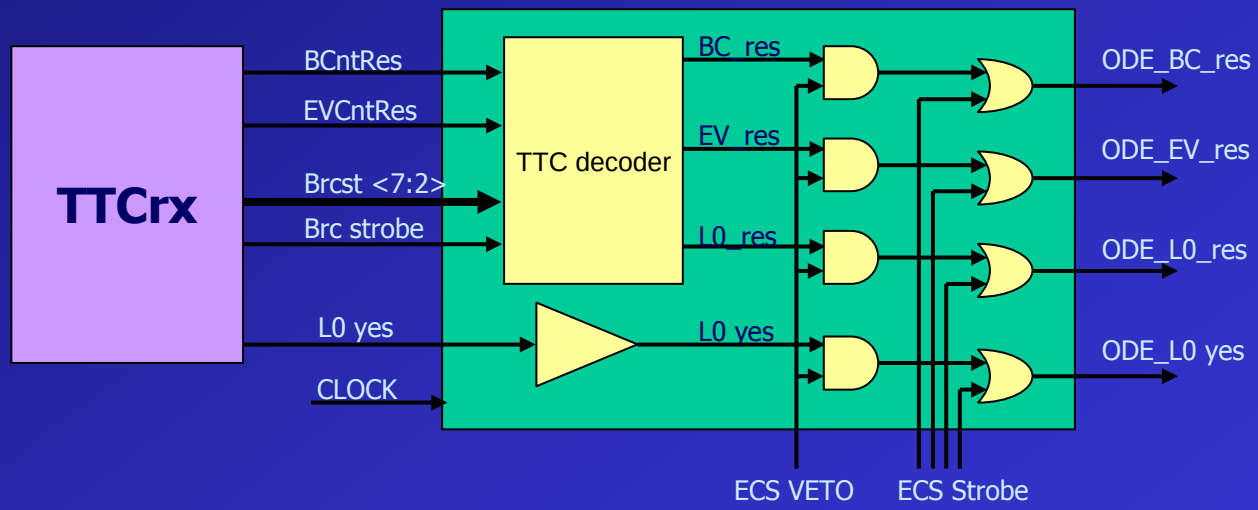


TTCrx and clock distribution

Paolo Ciambrone INFN- LNF

TTC system signals

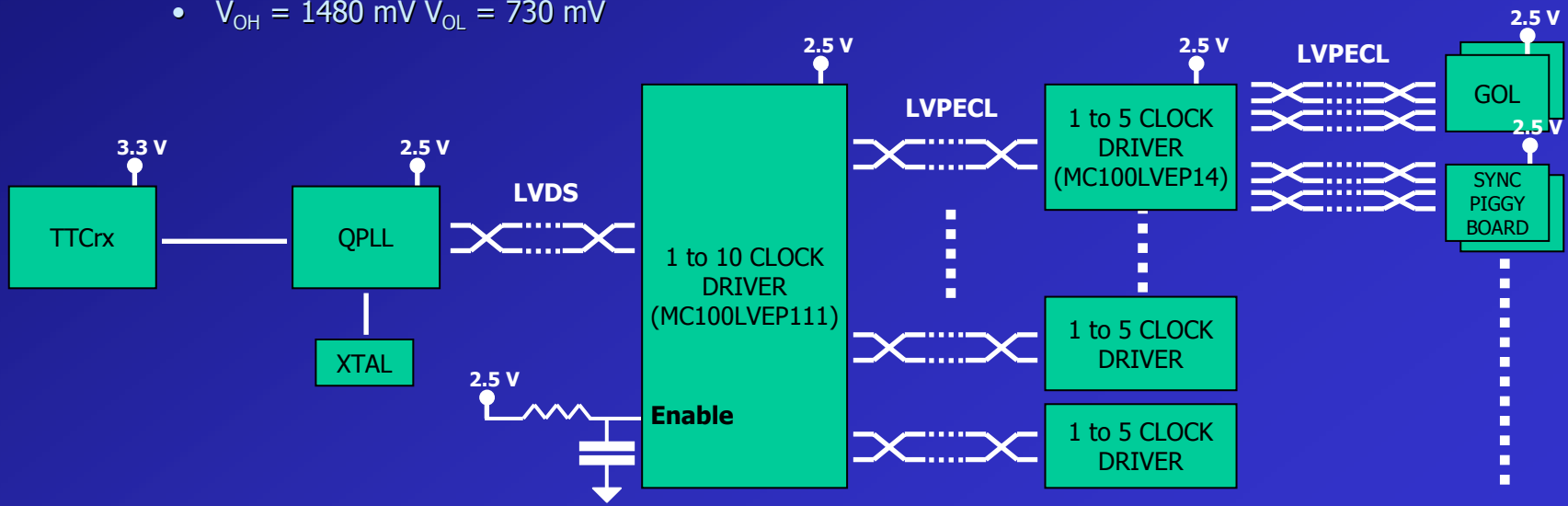
- TTC system interface is managed by the board controller
  - Receives signals from TTCrx
    - Decode broadcast command
      - Bunch-ID reset (BC_res) → Synchronous reset or preload for all ODE Bunch-ID counters
      - L0 Event ID reset (EV_res) → Synchronous reset for all ODE L0 Event-ID counters
      - L0 reset (L0_res) → Synchronous reset for all ODE L0 stages
  - Distributes L0 trigger and reset signals internally to the FPGA and to the SYNC chips
- The TTC reset signals do not modify the board configuration
  - No TTC resets delivered to GOL chips
  - ODE global reset (ODE default state) deliverable by ECS through ELMB



Paolo Ciambrone INFN- LNF

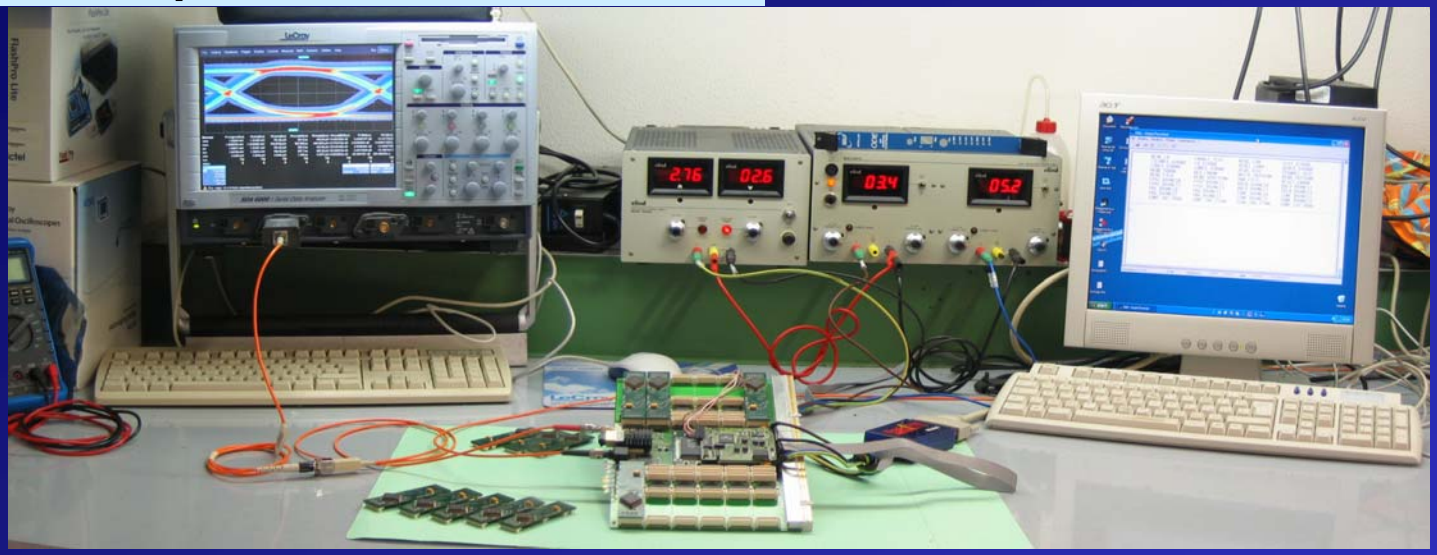
Clock distribution

- LHCb clock (40.08 MHz) is received through the TTCrx chip
  - The ODE is a completely synchronous system
- TTCrx recovered clock must be de-jittered
  - TTCrx jitter > 240 ps peak-to-peak
  - Maximum allowed GOL jitter is 100 ps peak-to-peak
- QPLL chip is used to reduce the jitter (< 50 ps peak-to-peak)
- Low jitter clock distribution tree (with enable)
  - MC100LVEP family @ 2.5 V
    - Jitter less than 1 ps RMS
    - 150 ps Typical Device-to–Device Skew (20 ps Typical Output-to-Output Skew)
  - LVPECL standard
    - V_{OH} = 1480 mV V_{OL} = 730 mV



Paolo Ciambrone INFN- LNF

Test setup



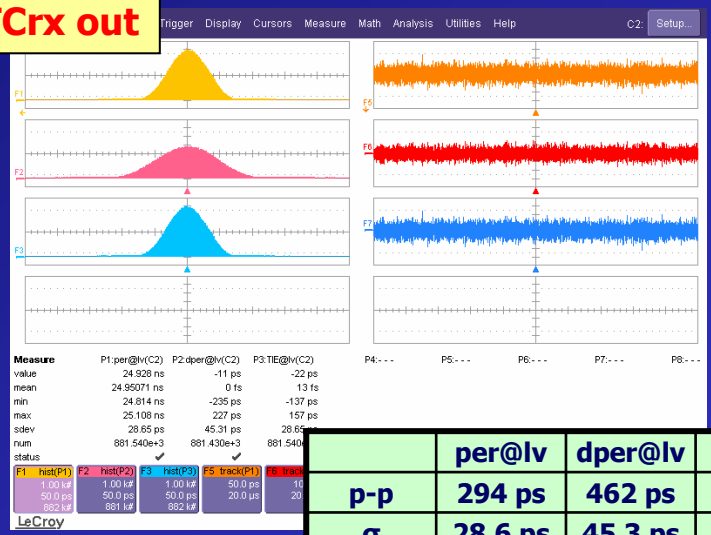
- LeCroy SDA6000 with active differential probe (LeCroy mod. D600AT)
  - 6 GHz Bandwidth
  - 20 Gsample/s on two channels
  - 1 ps rms trigger jitter
  - Analysis on continuous acquired data stream
    - Analysis on consecutive interval unit or cycle
    - Trigger jitter free
- Jitter measurements
  - Per@level
    - Period at a specified level for every cycle in the waveform
  - Dper@level
    - Adjacent cycle deviation at a specified level (cycle-to-cycle jitter) of each cycle in the waveform
  - TIE@level
    - Difference between the measured times of crossing a given level and the ideal expected time

Paolo Ciambrone INFN- LNF

Jitter measurements

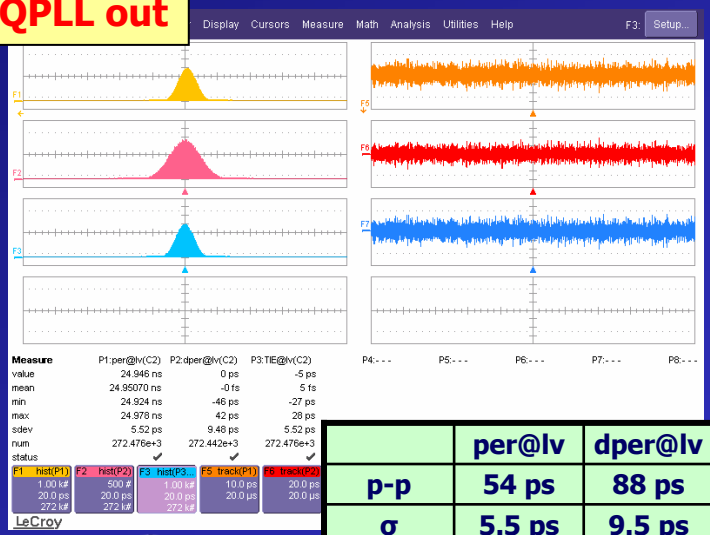
- Activity on both TTCrx channels via TTCvi + TTCvx boards:
  - ~ 20 MHz L0yes signal
  - ~ 400 KHz L0_res and EV_res signal
  - ~ 850 KHz BC_res signal
- Jitter at the GOL input well inside the specs
- Skew between clock lines < 300 ps

TTCrx out



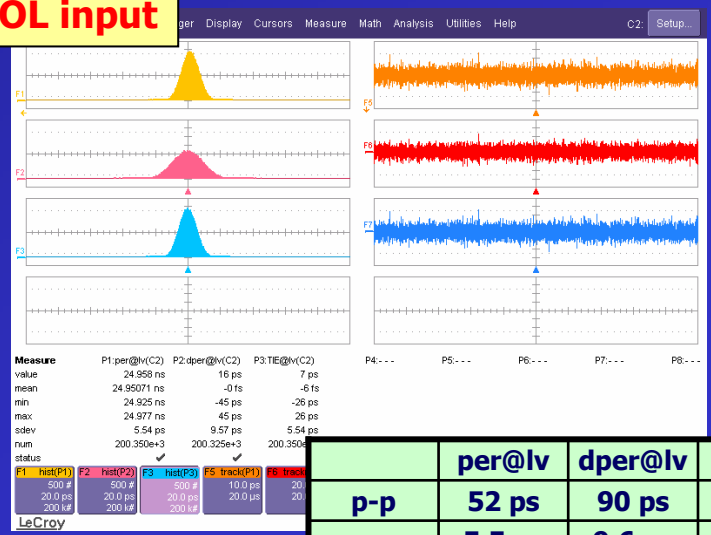
	per@lv	dper@lv	TIE@lv
p-p	294 ps	462 ps	294 ps
σ	28.6 ps	45.3 ps	28.6 ps

QPLL out



	per@lv	dper@lv	TIE@lv
p-p	54 ps	88 ps	55 ps
σ	5.5 ps	9.5 ps	5.5 ps

GOL input



	per@lv	dper@lv	TIE@lv
p-p	52 ps	90 ps	52 ps
σ	5.5 ps	9.6 ps	5.5 ps

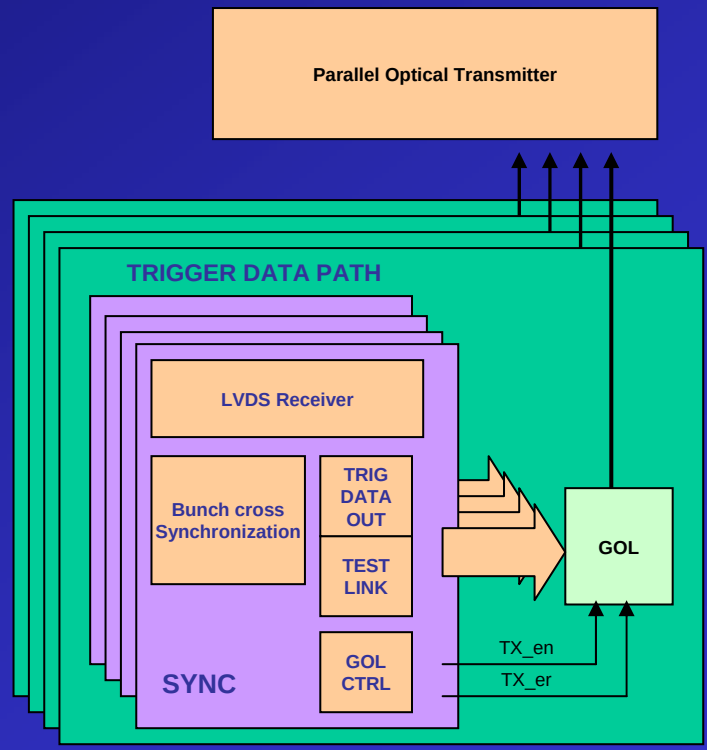
Paolo Ciambrone INFN- LNF

L0 Trigger interface

Paolo Ciambrone INFN- LNF

Trigger data flow

- Unidirectional data transfer to trigger system
  - Logical channels merging to produce Trigger Unit (TU)
- Each SYNC chip for every machine cycle (40 MHz)
  - Receives and synchronizes 8 input signals
  - Assigns correct Bunch Crossing identifier (BX_Id)
  - Produces 10 bit data output (8 hits + 2 LSB of BX_Id)
- 2,3 or 4 SYNC chips per Trigger Unit
- 1 GOL chip per Trigger Unit
  - Transmission (tx_en, tx_er) driven by one "master" SYNC
  - Fast Ethernet mode (8B/10B)
- 12 GOL chips drive a parallel optical link
  - 12 links @ 1.6 Gbit/s each
  - Agilent HFBR772
- Test link facilities
  - Fixed or pseudo-random pattern
    - Check link integrity
    - BER test



Paolo Ciambrone INFN- LNF

Trigger Unit type

- Trigger Unit configurations

Station	Region	Logical Channel per TU	SYNC per TU	Active channels per SYNC	TU per ODE (Active O.L.)	Active ODE Channels	# ODE
M1	R1 R2 R3 R4	24	3	8	8	192	12 12 12 12
M2 or M3	R1 R2 R3 R4	28 16 28 28	4 2 4 4	7 8 7 7	6 12 6 6	168 192 168 168	8 + 8 8 + 8 8 + 8 8 + 8
M4 or M5	R1 R2 R3 R4	24 14 10 10	3 2 2 2	8 7 5 5	8 12 12 12	192 168 120 120	6 + 6 4 + 4 4 + 4 4 + 4

- Minimizing number of different PCB
  - Optimize performances
  - Improve maintenance
- Unique motherboard for all TU
  - 12 piggy board slots
  - 12 GOL chips
    - 6 / 8 / 12 active optical links
- 3 different piggy boards (PB)
  - 24 SYNC per ODE
    - 2 / 3+3 / 4 SYNC per piggy board (Type 3/2/1)
    - 120 / 168 / 192 active input signals

Paolo Ciambrone INFN- LNF

Trigger data format

- Trigger data format
  - SYNC data merged on piggy board to produce TU
    - Up to 28 data bits
    - 2 LSB of BX_Id
    - 2 switch bits to ensure data alignment in the trigger system

	31			15			0
1st word	14 HIT DATA	0	1	14 HIT DATA	0	0	
2nd word	14 HIT DATA	0	1	14 HIT DATA	1	0	
3rd word	14 HIT DATA	1	1	14 HIT DATA	0	0	
4th word	14 HIT DATA	1	1	14 HIT DATA	1	0	

BX_Id bit

Switch bit

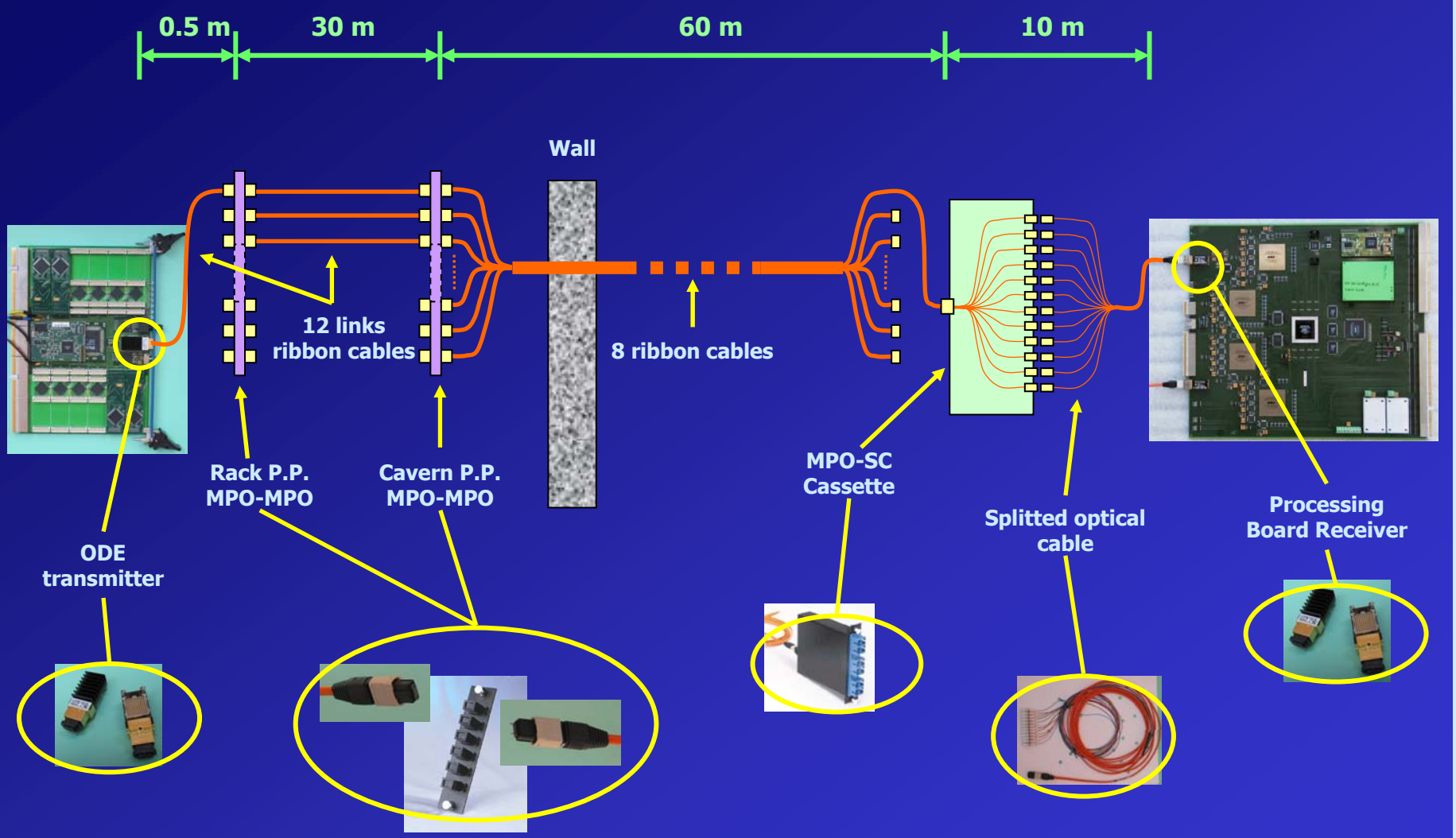
- PB type 1: 4 SYNC – 7 bits per SYNC → 28 bits per TU

- PB type 2: 3+3 SYNC – 8 bits per SYNC → 24 bits per TU

- PB type 3: 2 SYNC – 8/7/5 bits per SYNC → 16/14/10 bits per TU

Paolo Ciambrone INFN- LNF

Trigger optical link



Paolo Ciambrone INFN- LNF

Trigger link performances

- Agilent HFBR772 transmitter
  - Output optical power
    - -8 dBm min (-4 dBm typ)
  - Extinction Ratio
    - 6 dB min. (7 dB typ)
  - Total jitter
    - 120 ps_{p-p} max (60 ps_{p-p} typ)
- ~ 100 m fiber
  - 850 nm, 50/125 µm, multimode
  - 3.5 dB/Km (TIA/EIA 568-B)
- 4 connections
  - 0.75 dB per connection (TIA/EIA 568-B)
- Agilent HFBR782 receiver
  - Input optical power sensitivity
    - -16 dBm max (-18.5 typ)
  - Input optical power saturation
    - -2 dBm min (-1 dBm typ)

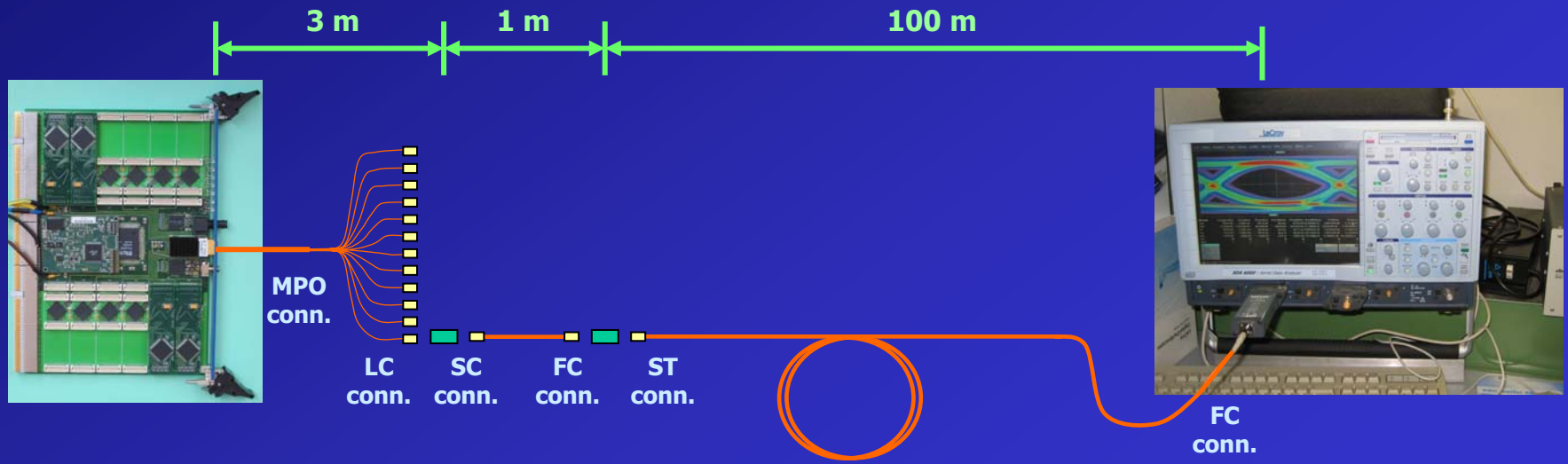
	Worst	Typ.	Unit
Output Optical Power	**-8**	**-4**	**dBm avg.**
Fiber attenuation	**0.35**	**0.35**	**dB**
Connectors attenuation	**3**	**3**	**dB**
Receiver input power	**-11.35**	**-7.35**	**dBm avg.**
Receiver sensitivity	**-16**	**-18.5**	**dBm avg.**
Power margin	**4.65**	**11.15**	**dB**

Paolo Ciambrone INFN- LNF

Test setup

- Optical to electrical converter (LeCroy mod. OE425)
  - 4.5 GHz Bandwidth (500 – 870 nm)
  - Conversion factor 0.5 V/mW (@ 800 nm) → slightly deviation @ 850 nm
  - FC2125 standard reference receiver
  - FC Golden PLL (digital) for clock recovery

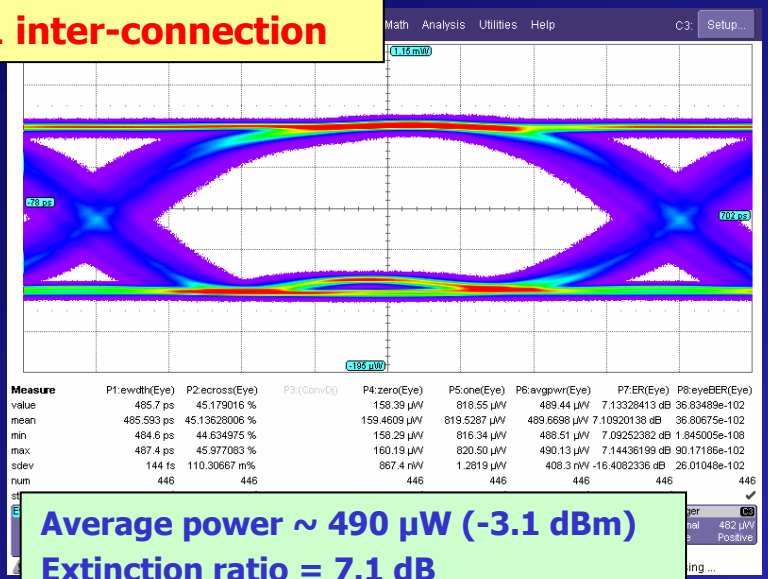
- Pseudo random bit sequence (2^8-1 bits)
  - 24 SYNC chips and 12 active GOL chips
    - 24 different seeds in PRBG
    - 16 input bits per GOL



Paolo Ciambrone INFN- LNF

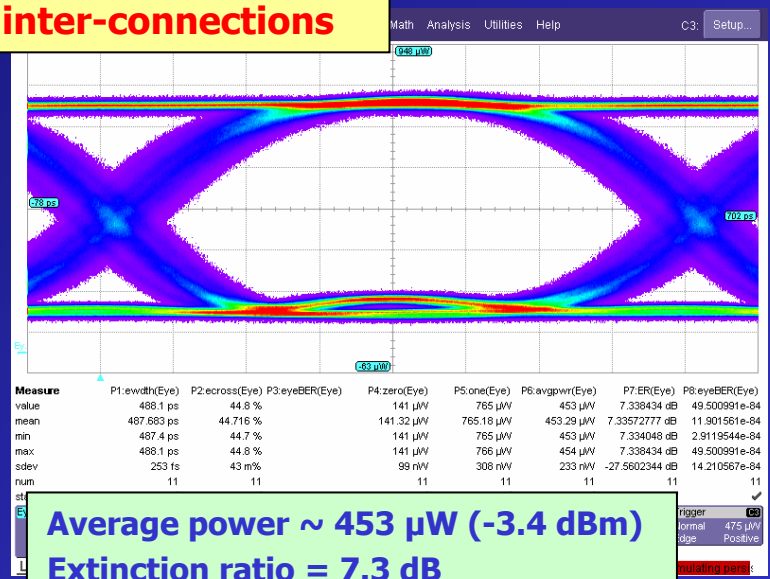
Eye Diagram

4 m fiber
1 inter-connection



Average power ~ 490 µW (-3.1 dBm)
Extinction ratio = 7.1 dB

~ 100 m fiber
2 inter-connections

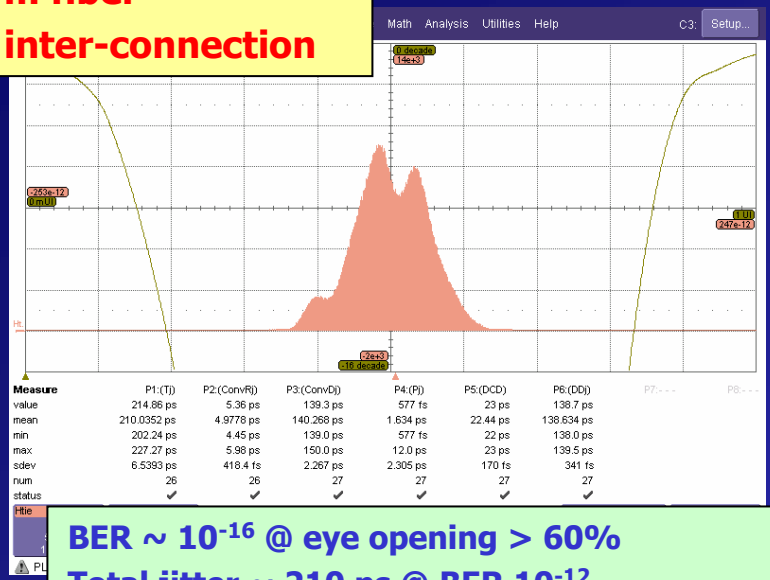


Average power ~ 453 µW (-3.4 dBm)
Extinction ratio = 7.3 dB

- Good datasheet agreement with short fiber
  - Average power → -4 dBm typ.
  - Extinction ratio → 7 dB typ.
- Well open horizontal and vertical eye diagram after 100m
  - Good extinction ratio
  - Good power margin (12.6 dB)
  - Low attenuation (0.3 dB)

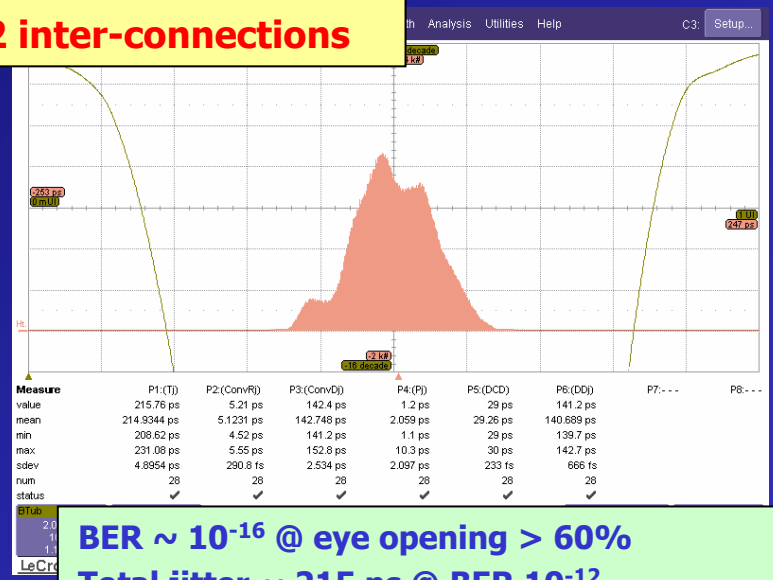
Bathtub curve

4 m fiber
1 inter-connection



BER ~ 10^{-16} @ eye opening > 60%
Total jitter ~ 210 ps @ BER 10^{-12}

~ 100 m fiber
2 inter-connections



BER ~ 10^{-16} @ eye opening > 60%
Total jitter ~ 215 ps @ BER 10^{-12}

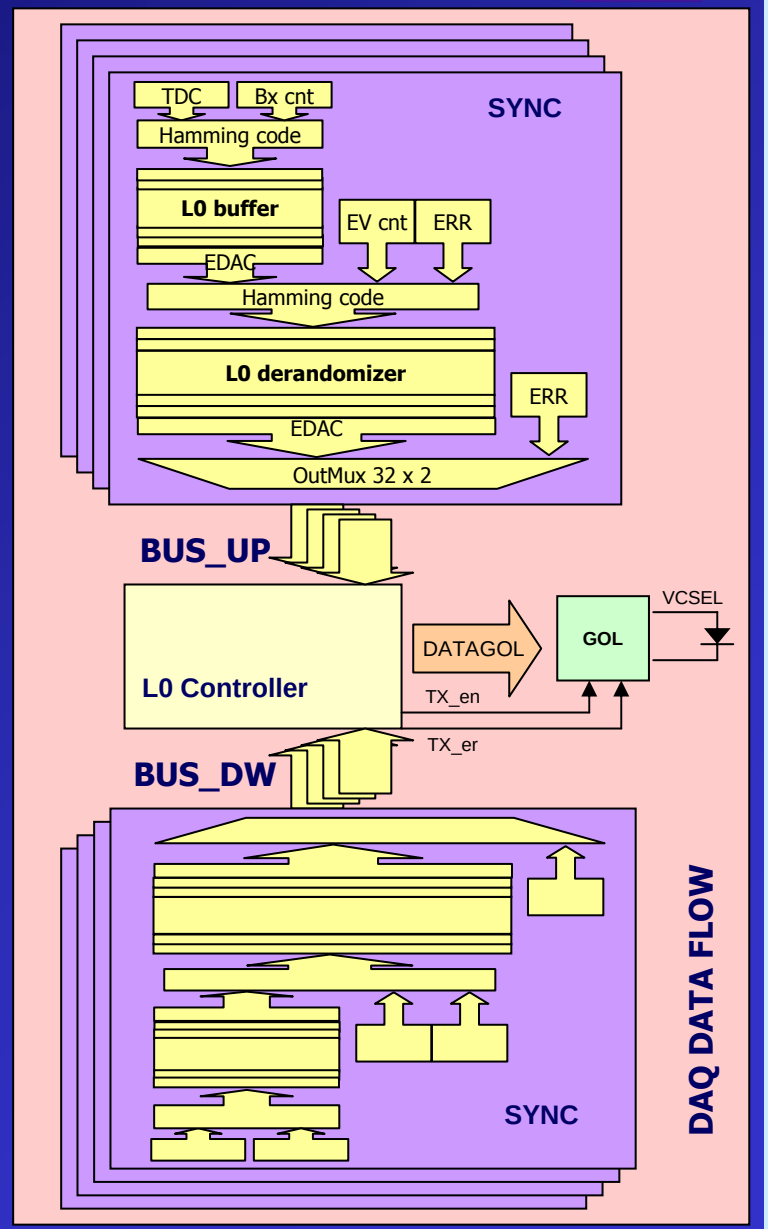
- Analysis on Time Interval Error
  - Estimated BER only on time jitter
- Estimated BER lower than 10^{-16} compatible with a 60% eye open
  - Deserializer TLK2501 guarantees 10^{-12} with a 50% eye opening
- Total jitter ~ 1/3 of UI dominated by deterministic component
- Real bit error test up to 10^{-12} with 99% confidence level

DAQ interface

Paolo Ciambrone INFN- LNF

DAQ data flow

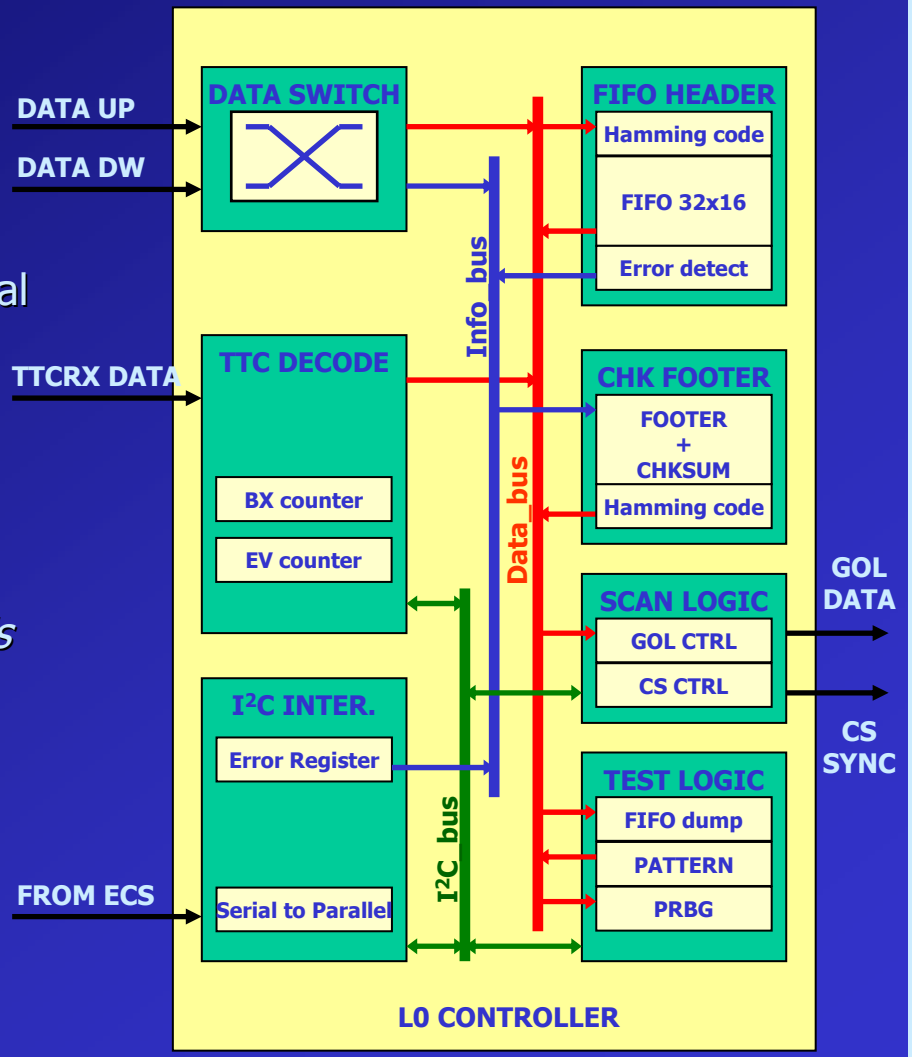
- Unidirectional data transfer to L1 DAQ
- SYNC chips
  - Measure input signal phase in LHCb clock period
    - 4-bit TDC with 1.6 ns resolution
  - Put data in L0 buffer (40 MHz)
  - Put data in L0 derandomizer after L0 trigger (1 MHz)
- SYNC data format
  - 32 bits for TDC data (*dataword*)
  - 32 bits for BX_Id, EV_Id, data error (*infoword*)
  - 32 bits output data bus
  - 24 SYNC X 2 accesses X 25 ns = 1200 ns > 900 ns
- Parallel SYNC readout mode
  - 2 x 32 bits wide buses (BUS_UP, BUS_DW)
  - 12 SYNC for each bus
- L0 controller
  - Reads data/info words from SYNC derandomizers
  - Creates L1 DAQ data frame
  - Drives GOL (tx_en, tx_er)
    - Ethernet mode (8B/10B)
    - VCSEL diode



Paolo Ciambrone INFN- LNF

L0 Controller

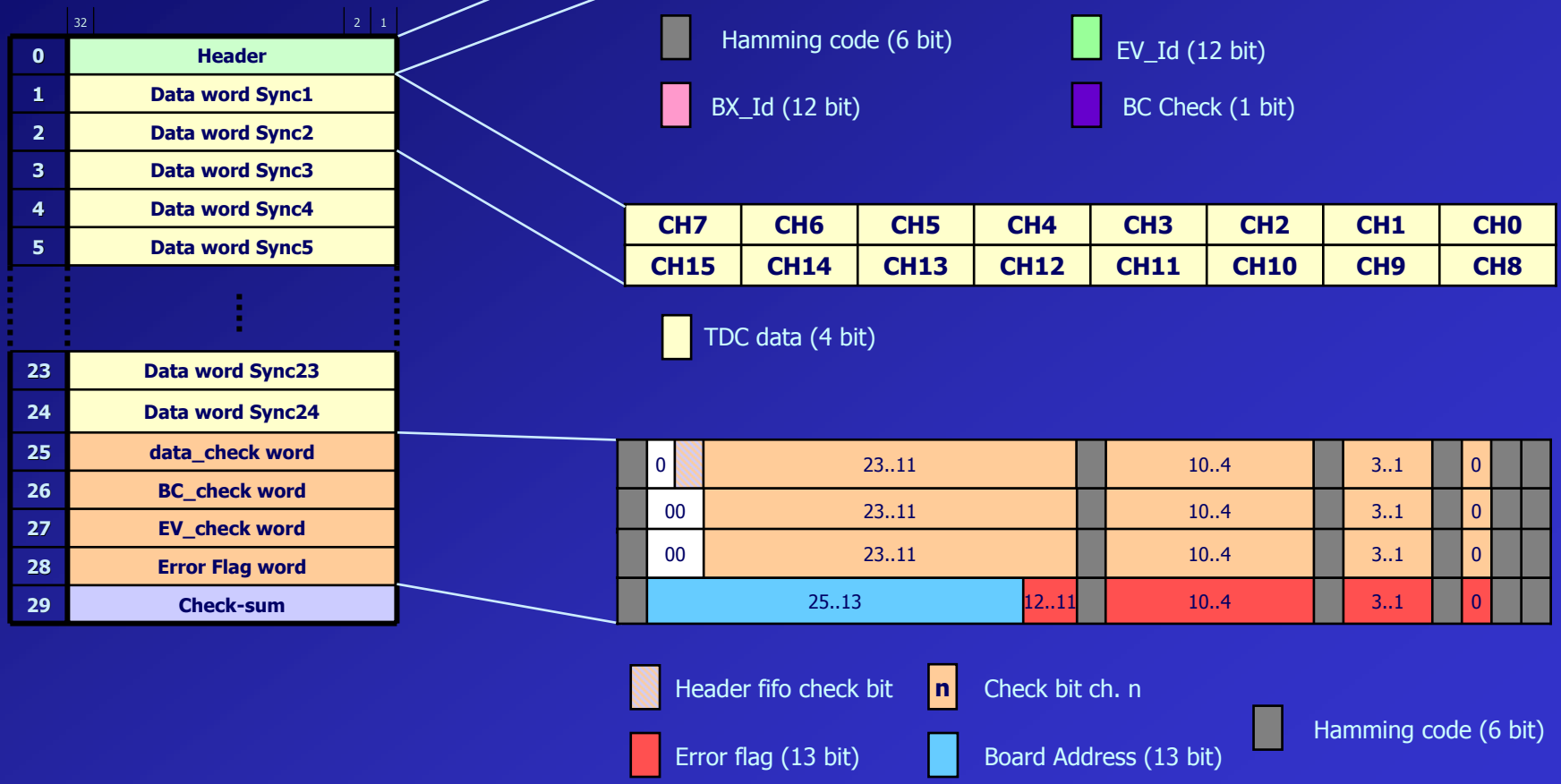
- Receives and decodes TTCrx data
- For each L0yes
  - Verifies TTCrx alignment
  - Generates a header word with internal BX_id and EV_id counters
  - Write the header in an internal FIFO
    - Up to 16 consecutive L0yes
- For each header word
  - Reads SYNC *datawords* and *infowords*
  - Verifies data alignment
  - Generates a footer words
  - Produces data frame for L1 DAQ
  - Drives GOL transmission
- Test facilities
- I²C interface



Paolo Ciambrone INFN- LNF

L1 data frame

- Data frame is preceded by an idle character
- Header and footer words hamming coded
- Data frame is 30 words long



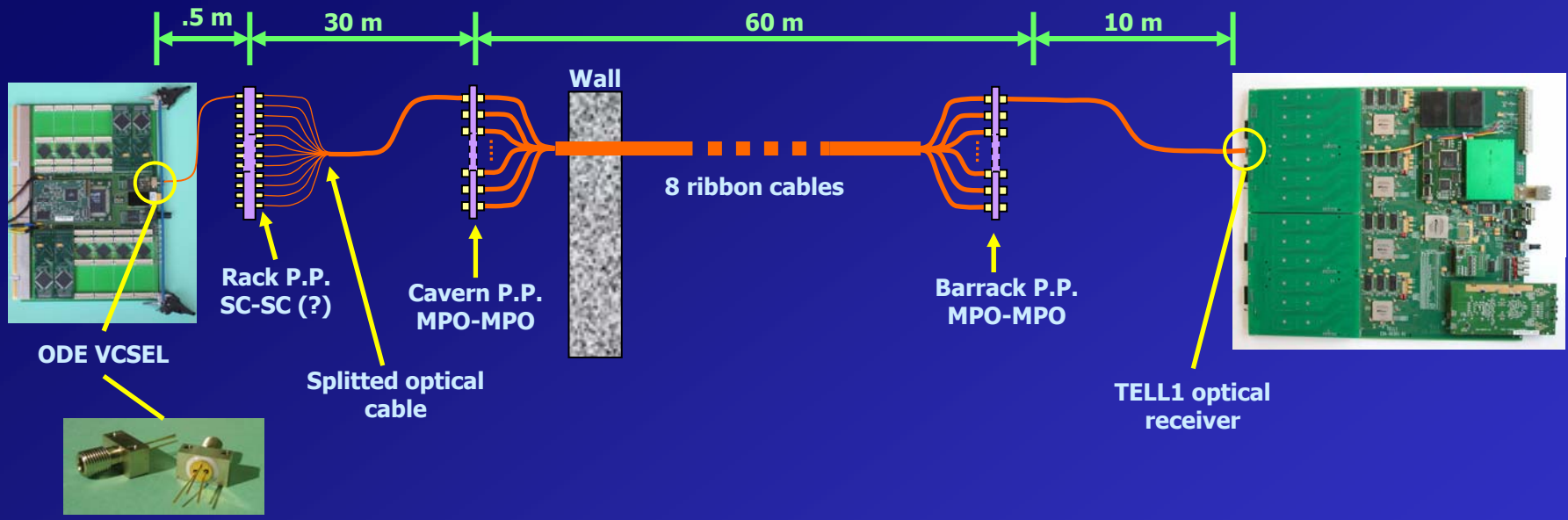
Paolo Ciambrone INFN- LNF

Test Facilities

- DAQ-SYNC Test Mode
  - Test DAQ data path
    - Known patterns loaded in SYNC L0 derandomizer via ECS
    - "Normal" data readout by board controller
- DAQ-Internal Test Mode
  - Test data link integrity and performances
    - Known patterns loaded in L0 board controller via ECS
    - 8 bits Pseudo-random sequence
- Trigger test mode
  - Test trigger link integrity and performances
    - Fixed pattern defined via ECS
    - 8 bits Pseudo-random sequence
- DAQ data dump
  - DAQ GOL frame dumped in a internal FIFO
  - DUMP mode programmable via ECS
- NO L0_YES needed in test mode
- All TTCrx signals emulated via ECS (L0_YES, BC_res, EV_res, L0_res)
- Error condition (TTCrx fault, DAQ GOL fault, SYNC error, etc.) stored in a STATUS register

Paolo Ciambrone INFN- LNF

DAQ link performances

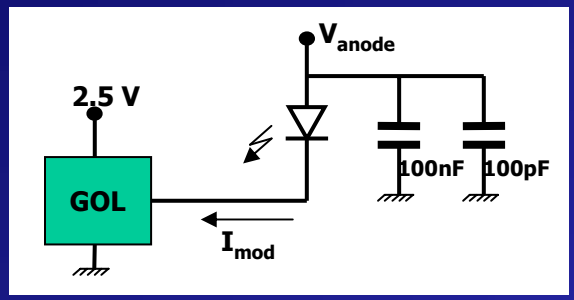


- Photonics VCsel ULM850-05-TN-USMBOP
  - 850 nm multimode VCsel
  - Forward laser voltage → V_F = 2 V
  - Threshold current → I_{th} = 1 mA
  - Slope efficiency → η = 0.1 W/A
  - Diff. series resistance → R_s = 60 Ω
  - SMA package
- ~ 100 m fiber
  - 850 nm, 50/125 μm, multimode
  - 3.5dB/Km (TIA/EIA 568-B)
- 3 (4) connections
  - 0.75 dB per connection (TIA/EIA 568-B)
- Receiver
  - Input optical power sensitivity
    - -16 dBm max (-18 typ)

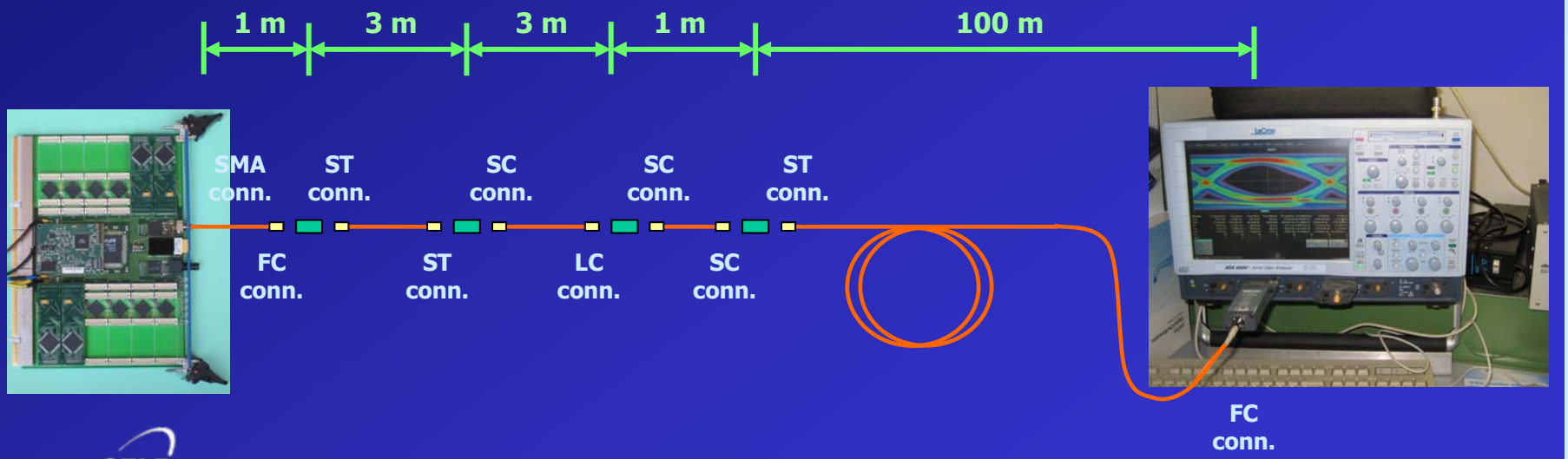
Paolo Ciambrone INFN- LNF

Test setup

- GOL driver specs
  - Programmable bias current
  - Fixed modulation current = 10 mA
    - '1' level → $I_{mod1} = I_{bias} + 10$ mA
    - '0' level → $I_{mod0} = I_{bias}$

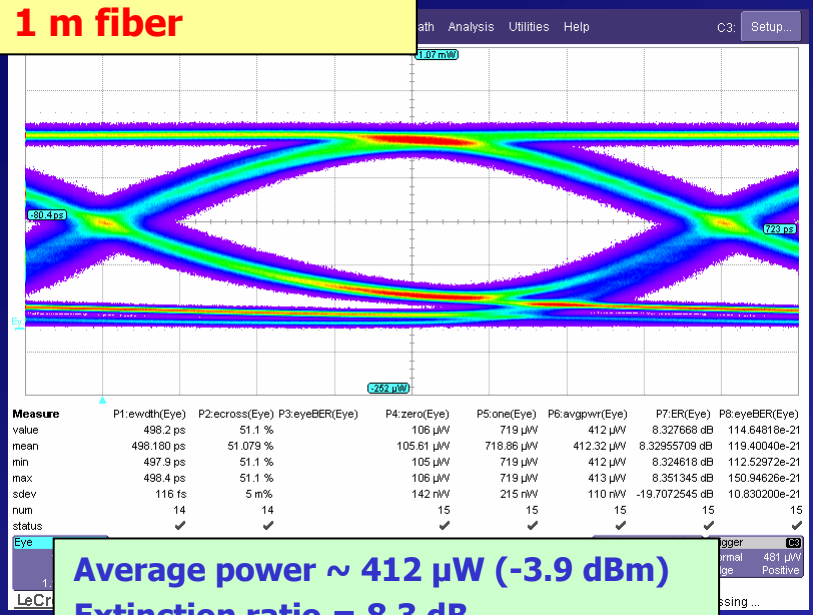


- I_{bias} = 1.8 mA
  - Maximum continuous current 12 mA
  - Laser threshold current 1 mA
- VCsel anode voltage = 3.3 V
  - GOL driver voltage >1 V
- FC2125 standard reference receiver
- FC Golden PLL (digital) for clock recovery
- Pseudo random bit sequence (2^{16}-1 bits)



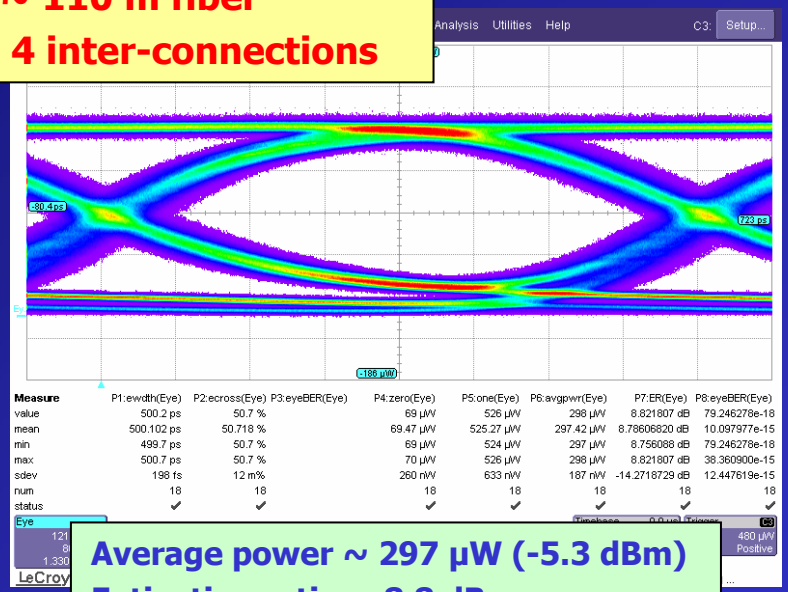
Eye diagram

1 m fiber



Average power ~ 412 µW (-3.9 dBm)
Extinction ratio = 8.3 dB

~ 110 m fiber
4 inter-connections



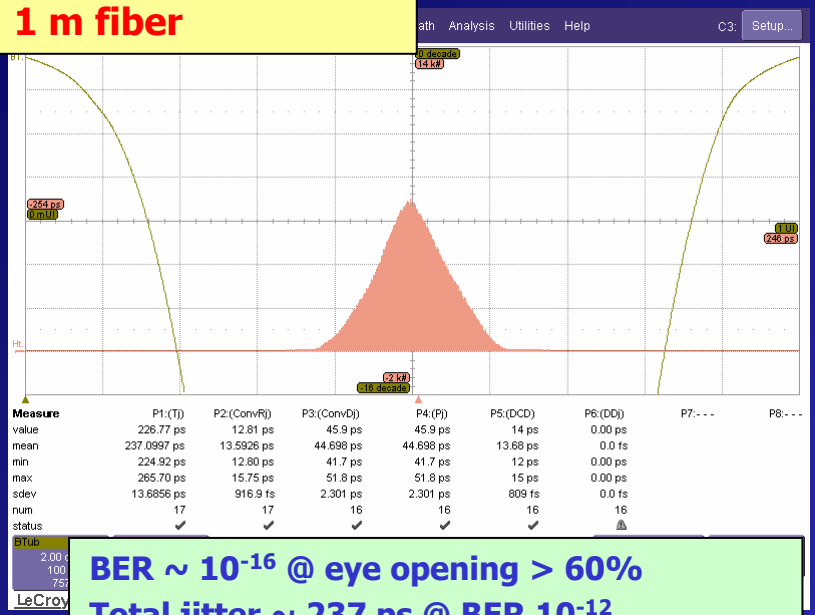
Average power ~ 297 µW (-5.3 dBm)
Extinction ratio = 8.8 dB

- Well open eye diagram
- Good extinction ratio
- Good power margin → 10.7dB worst (12.7 dB typ)
- Attenuation → 1.4 dB

Paolo Ciambrone INFN- LNF

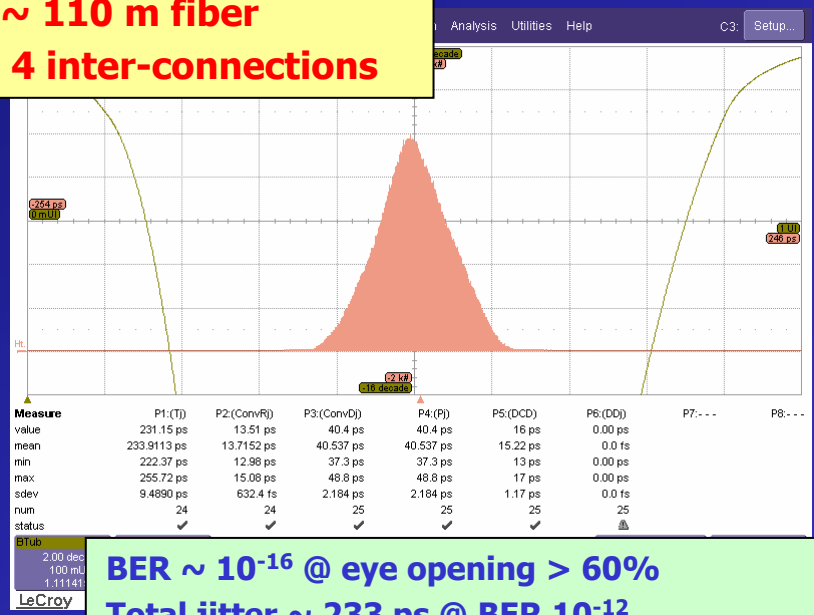
Bathtub curve

1 m fiber



BER ~ 10^{-16} @ eye opening > 60%
Total jitter ~ 237 ps @ BER 10^{-12}

~ 110 m fiber
4 inter-connections



BER ~ 10^{-16} @ eye opening > 60%
Total jitter ~ 233 ps @ BER 10^{-12}

- Estimated BER lower than 10^{-16} with 60% open eye
- Total jitter @ 10^{-12} ~ 1/3 UI
- Real bit error test up to 10^{-12} with 99% confidence level

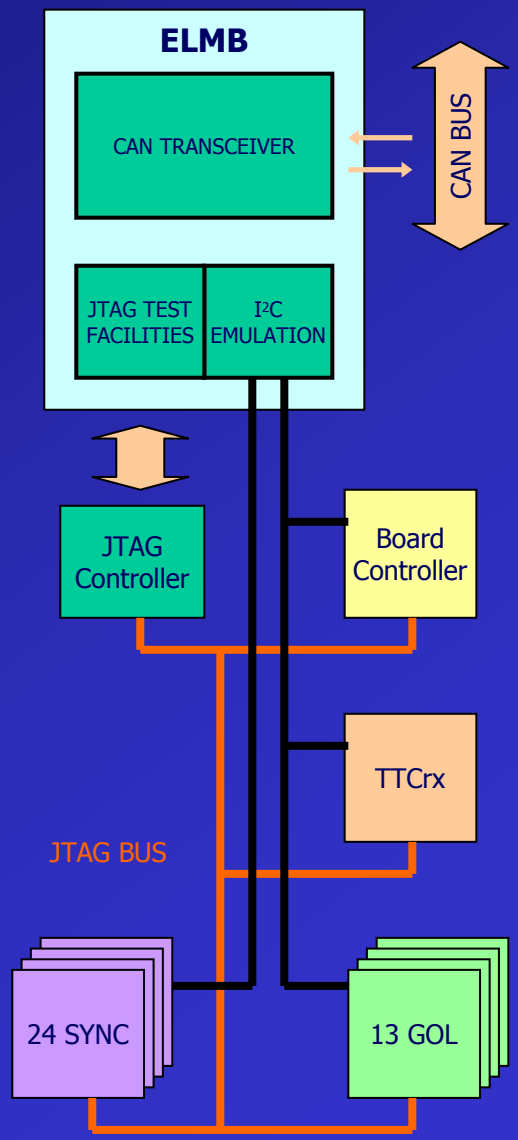
Paolo Ciambrone INFN- LNF

ECS interface

Paolo Ciambrone INFN- LNF

ECS interface

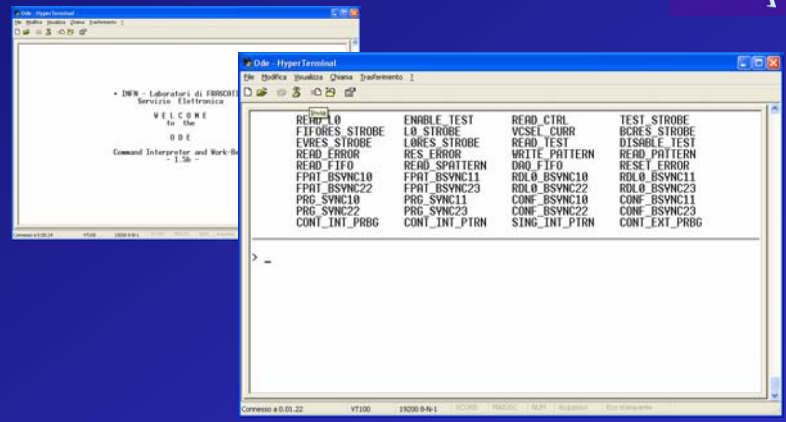
- ECS interface via ELMB card
  - ATmega128 µprocessor with CAN controller
  - CANbus line on backplane
    - 1 branch with up to 16 ODE
    - 2 branches with up to 10 ODE each
- ELMB on-board connection
  - Global reset
    - Startup (programmable)
    - ECS (only way to reset TTCrx and GOL after startup)
  - 2 I^2C bus
    - 24 SYNC
    - 13 GOL, TTCrx, L0 controller
    - Configuration, monitor, SYNC histogram read-out
  - 1 bus JTAG
    - Boundary scan
- CAN transceiver powered by ODE power supply
  - Optocoupler foreseen on the KVASER board (PCI-CAN interface) for galvanic isolation



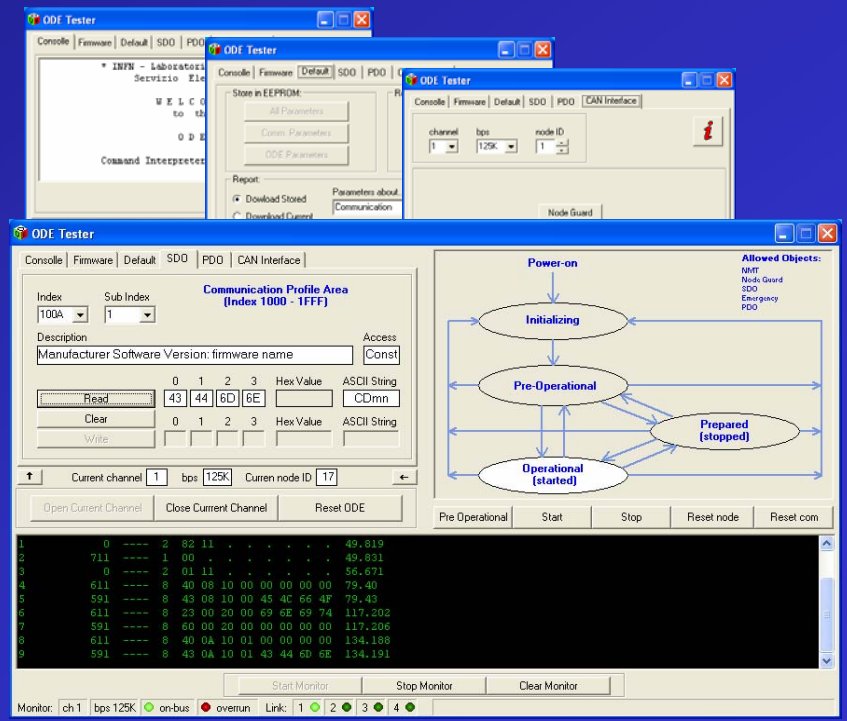
Paolo Ciambrone INFN- LNF

ELMB interface

- Serial interface for local access
  - RS232
  - Program on ELMB flash ram
    - Shell for command decoding



- CAN interface for remote access
  - CANopen standard protocol
  - ODE tester program
    - Single *Object Dictionary* access via SDO or PDO
    - Node status monitor and control
    - Bus traffic monitor
    - Scripting language console for high level command
    - CAN-JTag command translator (to be implemented)
  - PVSS console for ECS



Paolo Ciambrone INFN- LNF

GOL start-up problem

Paolo Ciambrone INFN- LNF

GOL start-up problem

- "It was observed by several users that the GOL might fail to start-up correctly. When that happens, a chip reset is not able to restore normal operation." [GOL manual]
- A brief history
  - If CLOCK arrives before complete GOL power-up …
    - Observed in the first ODE prototype
    - Enable on the clock network driven by 2.5 V
  - If the GOL is powered-up after other circuits that provide input signal to the GOL …
    - Never observed on the ODE board
    - ALL chip powered at 2.5 V with the exception of TTCrx, ELMB and VCsel
    - When 2.5V is OFF and 3.3V is ON the 2.5V power plane goes at ~700 mV
      - TTCrx (through FPGA input pin) partially power the 2.5V plane
      - This voltage should be not enough to power partially the GOL chip
  - If the power-up is too slow…
    - Never observed on the ODE board
    - Test power-up sequence with ramp-up ranging from 5 ms to 250 ms
      - First 3.3 V ON and then 2.5 V ON

Paolo Ciambrone INFN- LNF

GOL start-up problem

- The recommendations:
  - The power-up sequence must be validated for operating conditions identical to the ones to be used in the final systems …
    - We do not have the final power supply (Wiener Maraton)
    - Anyhow power-up sequence can be defined in the final power supply
  - Use CRT4T …
    - 13 GOL on the ODE motherboard
      - 13 chips
      - 13 control line
      - Also VCsel needed a CRT4T
    - Huge change in the layout !!!

It is really necessary?

Paolo Ciambrone INFN- LNF

Radiation hardness assurance

Paolo Ciambrone INFN- LNF

Muon Radiation Environment

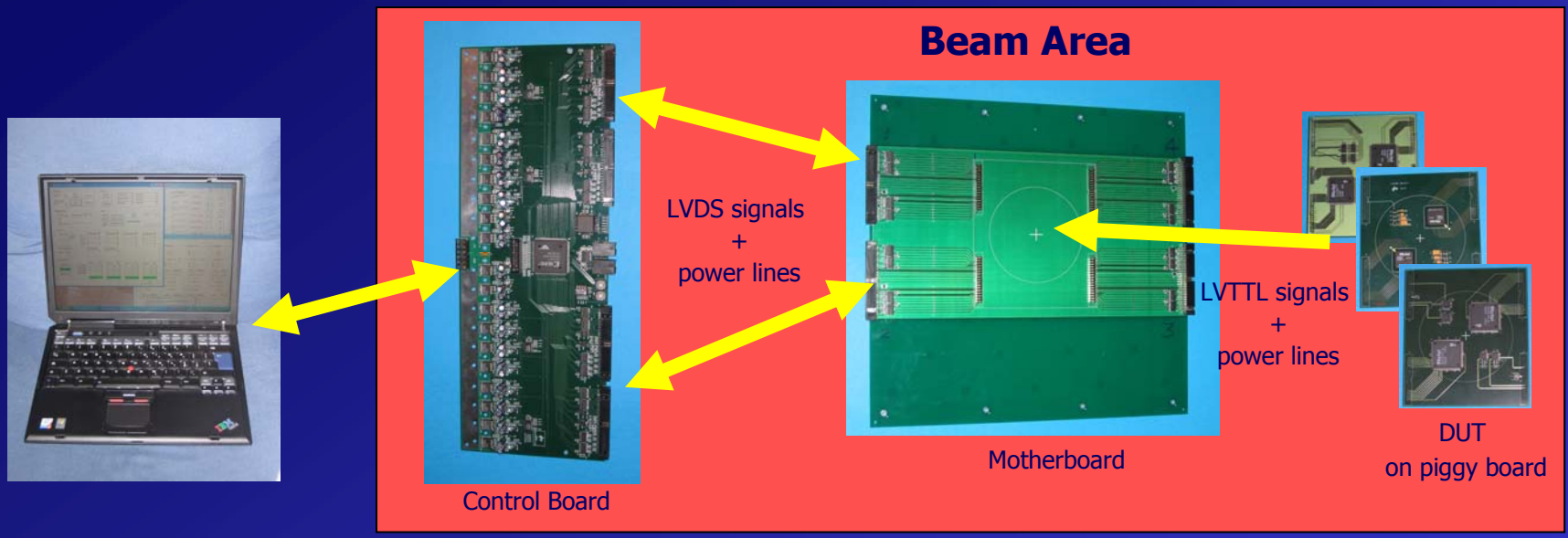
	Total dose (Rad) (10 years)	1 MeV Neutron eq. (10 years)	Hadrons > 20 MeV (10 years)
M1 (IB/ODE)	$7 – 7.9 \times 10^3$	$9 – 9.8 \times 10^{11}$	$4.3 – 5 \times 10^{10}$
M2 (IB/ODE)	$1.7 – 2.2 \times 10^3$	$3.2 – 3.4 \times 10^{11}$	$1.8 – 1.9 \times 10^{10}$
M3 (IB/ODE)	580 - 680	1.8×10^{11}	$7.3 – 7.9 \times 10^9$
M4 (IB/ODE)	180 - 390	$1.2 – 1.9 \times 10^{11}$	$2.6 – 5.3 \times 10^9$
M5 (IB/ODE)	130 - 320	$2.5 – 2.6 \times 10^{11}$	$4.3 – 4.5 \times 10^9$
Bunker	400 - 700	$5.6 – 9.6 \times 10^{11}$	$1.5 – 2.9 \times 10^{10}$

Component	Tested by	Tech.
GOL	CERN MIC	Rad-Tol
TTCrx	CERN MIC	Rad-Tol
QPLL	CERN MIC	Rad-Tol
SYNC	INFN-Cagliari	Rad-Tol
ELMB board	ATLAS	COTS
VCsel ULM850-05	LHCB ST	COTS
Agilent transmitter HFBR772	LHCb Muon Marseille	COTS
True-light PIN-preamp TRR-1B43-000	CERN	COTS
JTAG controller SN74LVT8980	ATLAS	COTS
Flash RAM AT45DB041B	LHCb Muon INFN-Roma1	COTS
Actel ProAsicPlus FPGA APA300	LHCb Muon INFN - LNF	COTS
Clock Driver MC100LVEP111	LHCb Muon INFN - LNF	COTS
Clock Driver MC100LVEP14	LHCb Muon INFN - LNF	COTS

- Safety factor 2 due to simulation included
- M1 now in a safer environment
- Total Integrated Dose (TID) of few Krad
  - Not a main concern in modern devices
- More stringent requirements for SEE and NIEL effect
  - Functional or destructive failures
    - SEL immune
  - Long term performances degradation

Paolo Ciambrone INFN- LNF

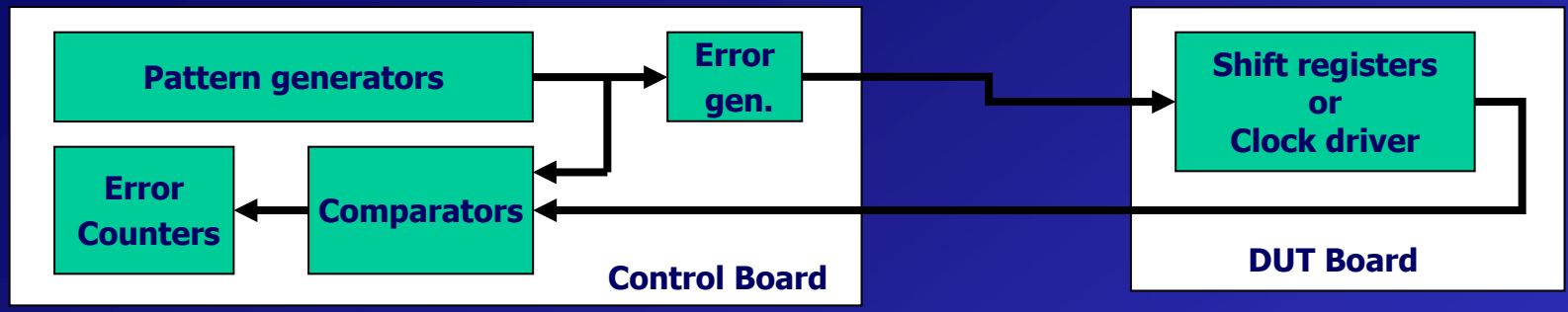
TEST setup



- DUT are mounted on three types of piggy board (up to 4 devices per board)
- Piggy boards are hosted on a single motherboard in the beam area
  - Control board and LVDS drivers/receivers are 2 meters away from the beam spot
- The control board allows:
  - To power DUT (3.3 V, 2.5V, 1.5V) via on board regulators
  - To monitor DUT I/O and core currents via 11 bit ADC (1 mA resolution)
  - To send known patterns to DUT and to receive DUT output signals
  - To verify sent and received patterns, counting the errors
  - To write and read DUT RAM blocks
  - To communicate via RS232 with a computer for settings, monitor and data readout

Paolo Ciambrone INFN- LNF

TEST logic



- FPGA Logic Test
  - 3 " regular" shift registers + 1 "TMR" shift register implemented in the FPGA
    - 1024 bit shift registers in APA FPGA (75% of flip-flops)
  - 3 different patterns used
    - "0", "1" pattern to verify different sensitivity
    - "01" pattern to verify clock upset and control logic upset
  - Shift register clocked at 1 MHz
  - Error forced every 2^{24}-1 bits for self-testing
  - I/O and Core current monitored

»

- FPGA RAM test
  - Static test comparing pre-irradiation and post-irradiation memory bit maps
  - APA SRAM block configured as 1x4096 bit
- Clock Driver Test
  - Clock at 1 MHz
  - 1 output channel per device observed

Paolo Ciambrone INFN- LNF

Beam parameter

- Proton beam at Louvain la Neuve Cyclotron
- Energy: ~ 70 MeV
- Beam size: 9 cm ∅
- 4 devices irradiated
- Nominal flux used
  - 5 x 10^{7} protons cm^{-2} s^{-1} up to 10^{11} protons cm^{-2}
  - 5 x 10^{8} protons cm^{-2} s^{-1} up to 6 x 10^{11} protons cm^{-2}
- Fluence of 6 x 10^{11} protons cm^{-2} correspond to:
  - ~ 6 x 10^{11} "energetic" hadrons (~ 200 years of LHCb muon life)
  - ~ 68.5 krad of TID (~ 300 years of LHCb muon life)
  - ~ 9 x 10^{11} neutrons cm^{-2} for NIEL (~ 10 years of LHCb muon life)

APA test data

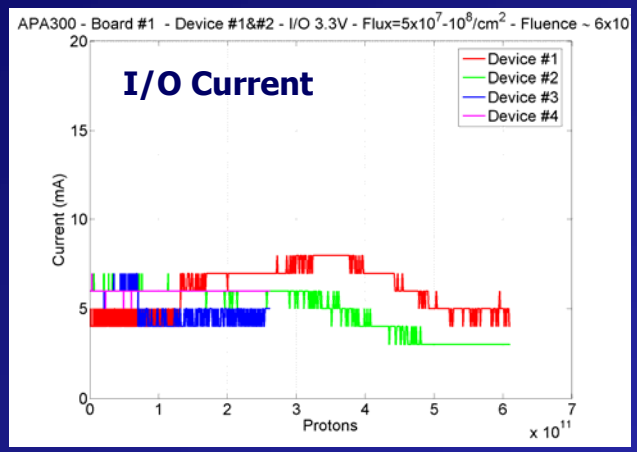
	Device A			Device B			Device C			Device D		
Fluence p/cm^2	"0" pattern	"1" pattern	"01" pattern	"0" pattern	"1" pattern	"01" pattern	"0" pattern	"1" pattern	"01" pattern	"0" pattern	"1" pattern	"01" pattern
10^{11}	0	1	2	0	5	2	1	4	3	0	5	1
2 x 10^{11}	0	5	1	2	0	3	0	2	7	2	3	4
3 x 10^{11}	2	3	4	5	2	2	2	2	1	1	4	2
4 x 10^{11}	-	-	-	-	-	-	2	2	3	0	4	4
5 x 10^{11}	-	-	-	-	-	-	2	4	4	0	0	5
6 x 10^{11}	-	-	-	-	-	-	1	1	1	0	0	1
TOT	2	9	7	7	7	7	8	15	19	3	16	17
σ_{bit} (10^{-14})	0.65	2.9	2.3	2.3	2.3	2.3	1.3	2.4	3.1	0.5	2.6	2.8

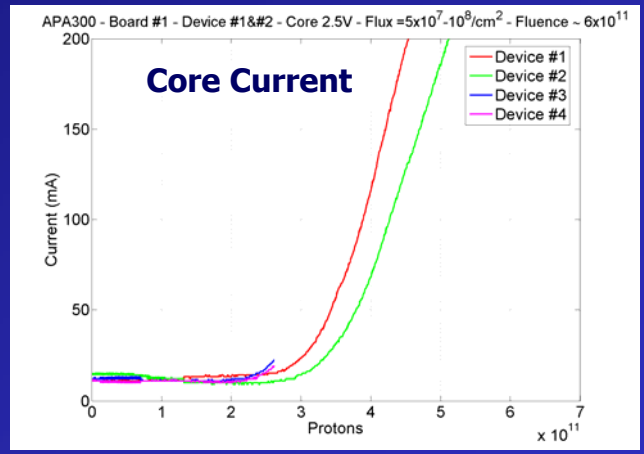
- Low SEU cross section per bit → ~ 10^{-14}
  - "1" pattern slightly more sensitive (?)
- No SEU in TMR shift registers
- No clock or control logic upset observed
- No SEL detected

Paolo Ciambrone INFN- LNF

APA test data

- Core current start to increase at a fluence of 2.5 x 10^{11} protons/cm^2 (~ 35 krad)
  - Devices continue to work





- SEU RAM cross section per bit ~ 10^{-13}

	Device A	Device B	Device C	Device D
Fluence p/cm^2	Ram Upset	Ram Upset	Ram Upset	Ram Upset
10^{11}	**27**	**40**	**38**	**42**
2 x 10^{11}	**53**	**30**	**-**	
6 x 10^{11}	**-**	**-**	**153**	**199**
TOT	**80**	**70**	**191**	**241**
σ bit (10^{-14})	**9.7**	**8.5**	**7.8**	**9.8**

Paolo Ciambrone INFN- LNF

Clock Driver test data

- MC100LVEP111
  - No SEU observed up to a fluence of 6 x 10^{11} protons/cm^2
    - Cross section per bit < 8.3 x 10^{-13} cm^2 $protons^{-1}$ bit^{-1}
  - No SEL detected
  - No current change @ 6 x 10^{11} protons/cm^2
- MC100LVEP14
  - 7 SEU observed with a fluence of 6 x 10^{11} protons/cm^2
    - Cross section per bit = 5.8 x 10^{-12} cm^2 $protons^{-1}$ bit^{-1}
  - No SEL detected
  - No current change @ 6 x 10^{11} protons/cm^2

Paolo Ciambrone INFN- LNF

ODE components

Component	Tested by		TID	SEE	reference
GOL	CERN MIC	Rad-Tol			
TTCrx	CERN MIC	Rad-Tol			Proceedings of the 6th Workshop on Electronics for LHC Experiments
QPLL	CERN MIC	Rad-Tol			http://www.cern.ch/proj-qpll/images/qpll2IrradData.pdf
SYNC	INFN - Cagliari	Rad-Tol			Note in preparation
ELMB board	ATLAS	COTS	**14 krad**	**6 x 10^{12} n/cm^2 (1 MeV equivalent)** **1 x 10^{11} p/cm^2 (60 MeV)**	ATLAS Internal Working Note DCS- IWN20, DCS- IWN21, DCS- IWN23
VCsel ULM850-05	LHCB ST	COTS	**300 krad**	**3.6 x 10^{12} n/cm^2 (1 MeV equivalent)**	LHCb note 2004-037
Agilent transmitter HFBR772	LHCb Muon Marseille	COTS	**15 krad**	**2.5 x 10^{11} p/cm^2 (250 MeV)**	LHCb note 2004-013
True-light PIN-preamp TRR-1B43-000	CERN	COTS	**1 Mrad**	**7 x 10^{13} n/cm^2 (1 MeV equivalent)** **1.2 x 10^{11} p/cm^2 (60 MeV)**	Proceedings of the 9th Workshop on Electronics for LHC Experiments,
JTAG controller SN74LVT8980	ATLAS	COTS	**30 krad**	**2.3 x 10^{11} p/cm^2 (70 MeV)**	http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard_MUON_TGC.htm
Flash RAM AT45DB041B	LHCb Muon INFN - Roma1	COTS	**20 krad**	**2 x 10^{11} p/cm^2 (60 MeV)**	Note in preparation
Actel ProAsicPlus FPGA APA300	LHCb Muon INFN - LNF	COTS	**68 krad**	**9 x 10^{11} n/cm^2 (1 MeV equivalent)** **6 x 10^{11} p/cm^2 (70 MeV)**	Note in preparation
Clock Driver MC100LVEP111	LHCb Muon INFN - LNF	COTS	**68 krad**	**9 x 10^{11} n/cm^2 (1 MeV equivalent)** **6 x 10^{11} p/cm^2 (70 MeV)**	Note in preparation
Clock Driver MC100LVEP14	LHCb Muon INFN - LNF	COTS	**68 krad**	**9 x 10^{11} n/cm^2 (1 MeV equivalent)** **6 x 10^{11} p/cm^2 (70 MeV)**	Note in preparation

- NO SEL detected
- No performances degradation observed for NIEL

Paolo Ciambrone INFN- LNF

SEE estimation…

- FPGA Hard SEE
  - Possible ODE permanent damage
  - Main worry in the first flash-based FPGA
  - From Actel tests no latch-up has been observed for LET higher than 100 MeV cm^2/mg for APA FPGA
  - This threshold should guarantee our system free from SEL
- FPGA SOFT SEE
  - Possible loss of ODE functionalities
  - 148 FPGA in the muon L0 electronics
  - Each FPGA uses
    - ~ 2000 flip-flops (without TMR)
    - 512 RAM bit
  - In the worst case
    - $3 \times 10^{-14} \times 5 \times 10^{10} \times 2000 \times 148 = 444$ flip-flop upsets in 10 years
    - $10^{-13} \times 3 \times 10^{10} \times 512 \times 148 = 227$ RAM bit upsets in 10 years
    - The foreseen TMR technique and EDAC coding allow to improve system reliability
- Clock Upset
  - Possible ODE misalignment and GOL loss of lock
  - 6 MC100LVEP14 (4 channels) per ODE (148 board)
    - $5.8 \times 10^{-12} \times 5 \times 10^{10} \times 4 \times 6 \times 148 = 1030$ upsets in 10 years

Paolo Ciambrone INFN- LNF

SEE estimation…

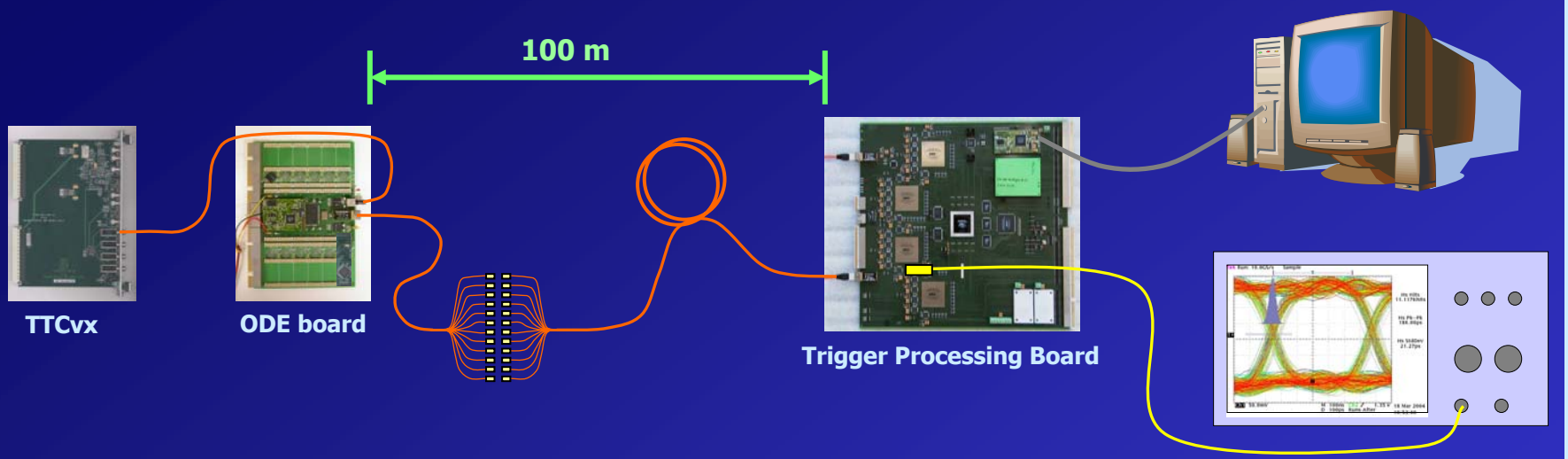
- HFBR772 upset
  - "The cross-section for single event upsets is equal to $(4.5\pm0.1)\times10^{-10}cm^2$ per single optical link. The corresponding inefficiency on the level-0 muon trigger is below 10^{-10} and therefore negligible." [LHCb note 2004-013]
- GOL, TTCrx, QPLL and SYNC upset
  - Rad-Tol technology
  - Negligible effect
- ELMB upset
  - Loss of ECS communication
  - No functional problems on the ODE (!)
  - ELMB can be reset through
    - Internal watchdog system
    - A "reset board" seated in the crate and controllable by ECS
- JTag controller and Flash Ram upset
  - No functional problems on the ODE

Paolo Ciambrone INFN- LNF

TEST ...

Paolo Ciambrone INFN- LNF

ODE – L0 muon trigger test



- ODE (first prototype) and the muon trigger processing board with 100 m ribbon fiber
- System clock generated by a TTCvx
  - Telecom frequency (77.76 MHz)
  - Maxim PLL+VCXO for clock de-jitter
- Data generated by the SYNC chips using their test features
  - Transmission of consecutive IDLE words
  - Transmission of fixed patterns wrote on SYNC through I^2C interface
  - Transmission of a Pseudo-random pattern generated on SYNC
- Received Data monitored on a PC and oscilloscope TDS694C
  - Check data integrity and synchronization
  - Well open eye diagram
  - Max peak-to-peak jitter 186 ps ($\sigma \sim 21$ ps)

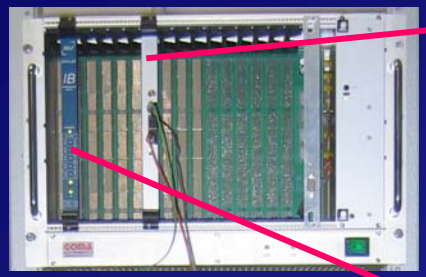
Paolo Ciambrone INFN- LNF

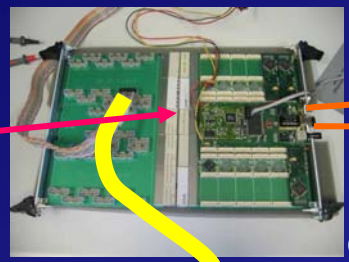
System Test

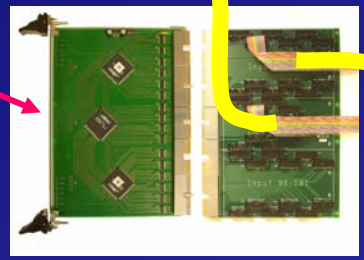
- 1 Muon Chamber
  - 12 CARDIAC (96 channels)
- 1 IB (+ TB) on custom crate
- 1 ODE (+ TB) on custom crate
- 1 VME crate with
  - 1 SB
  - 1 TTCvx
  - 1 TTCvi
  - Clock generator (custom) board
  - Optical Receiver board (custom)
  - 1 interface VME-PCI
- Control PC with
  - PVSS
  - KVASER board (PCI-CAN interface)
  - ODE control software
- Pattern generator and Logic Analyzer

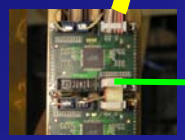
Paolo Ciambrone INFN- LNF

Chain setup


Custom crate

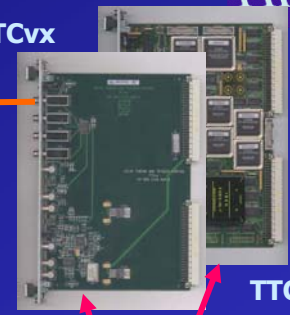

ODE + TB


IB + TB

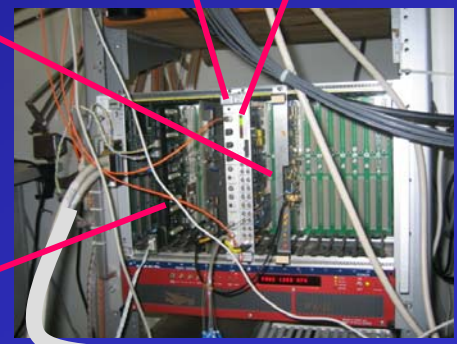

CARDIAC

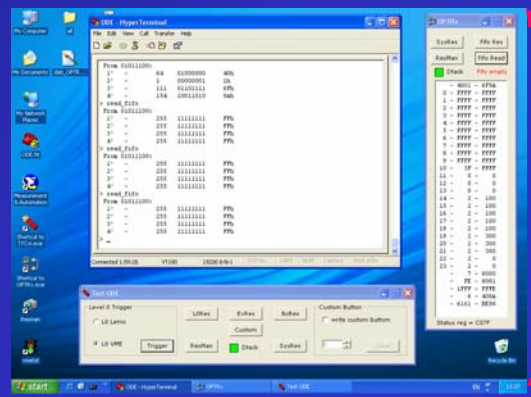

Optical receiver

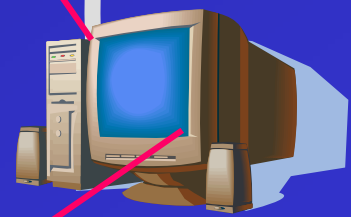

SB


TTCvx

TTCvi


VME crate





Paolo Ciambrone INFN- LNF

Test performed

- TTC interface
  - TTC command (L0yes, L0_res, BC_res, Ev_res) sent using TTCvi+TTCvx
  - Command correctly received, decoded and distributed on the ODE
- Front-end, trigger and DAQ interfaces
  - Using the pulse functionality on SB and DIALOG,
    - generate specific DIALOG inputs and find them in the right place at the end of the chain
    - generate specific DIALOG inputs put in specific logical combination among them and find the right logical channel (only) in the right place at the end of the chain. 2 kinds of combinations were possible:
      - 2 logical channels starting from 4 physical channels (2xOR2)
      - 1 logical channel starting from 4 physical channels (1xOR4)
  - Data checked directly at the end of the chain following the 2 possible data links (Trigger and DAQ)
    - Both checks performed by reading data on a FIFO in the optical receiver board
    - Verifying correctness of data frame and synchronization
- ECS interface
  - ODE configuration
  - SYNC histogram read-back

Paolo Ciambrone INFN- LNF

Production test

- Quality assurance on board assembly (factory)
- TTC interface test
  - TTCvi + TTCvx
  - Synchronization and command decoding test
- Front-end input test
  - SYNC chip already tested
  - Patter generator or random pulses
  - Histogram from SYNC
- Trigger and DAQ link test
  - BERT up to 10^{-12} using ODE test features
  - Custom 6U VME board
    - 8 full duplex optical channel
    - VirtexIIPRO
      - 8 full duplex serial transceivers @3.125 Gbit/s
      - IBM 400MHz PowerPC™
      - 400 MHz clock rate
    - TTCrx + QPLL for system synchronization
    - 528 Kbytes fast dual port RAM
- ECS interface test
  - Board initialization and test via CANbus interface

Paolo Ciambrone INFN- LNF

Conclusions

- ODE board fully characterized
  - Architecture well defined
  - Low jitter clock network
    - 50 ps peak-to-peak
  - Low BER optical links for trigger and DAQ
    - 10^{-16} estimated BER
    - 10^{-12} measured BER
  - Good radiation hardness assurance

- ODE board fulfils the experiment requirements
  - L0 requirements
    - Buffering, consecutive triggers, alignment check, test features, …
  - Trigger and DAQ systems requirements
    - Formatting, transmission quality, …

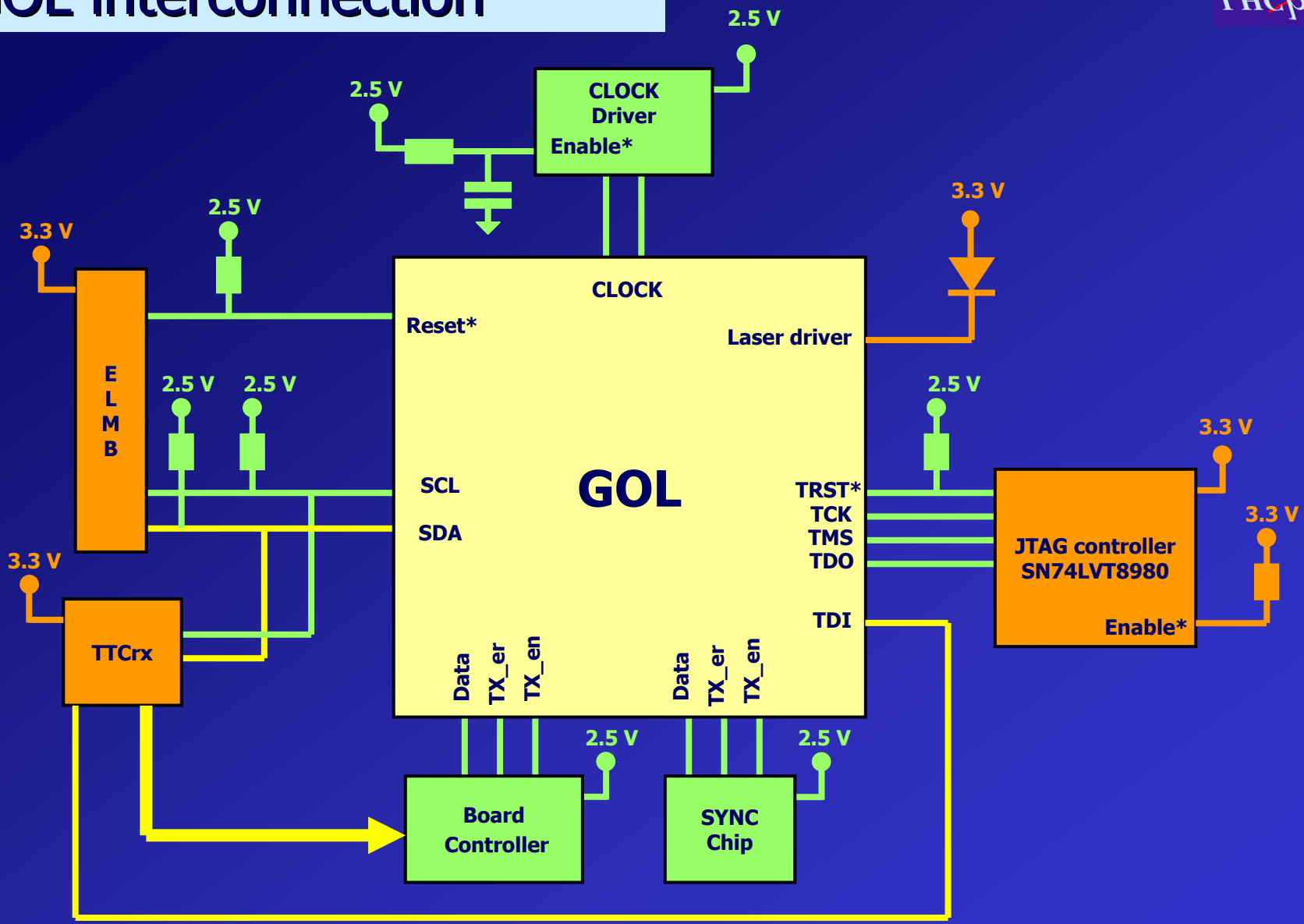
- Ready for the pre-production
  - Production test-stand defined

Paolo Ciambrone INFN- LNF

Spare slides

Paolo Ciambrone INFN- LNF

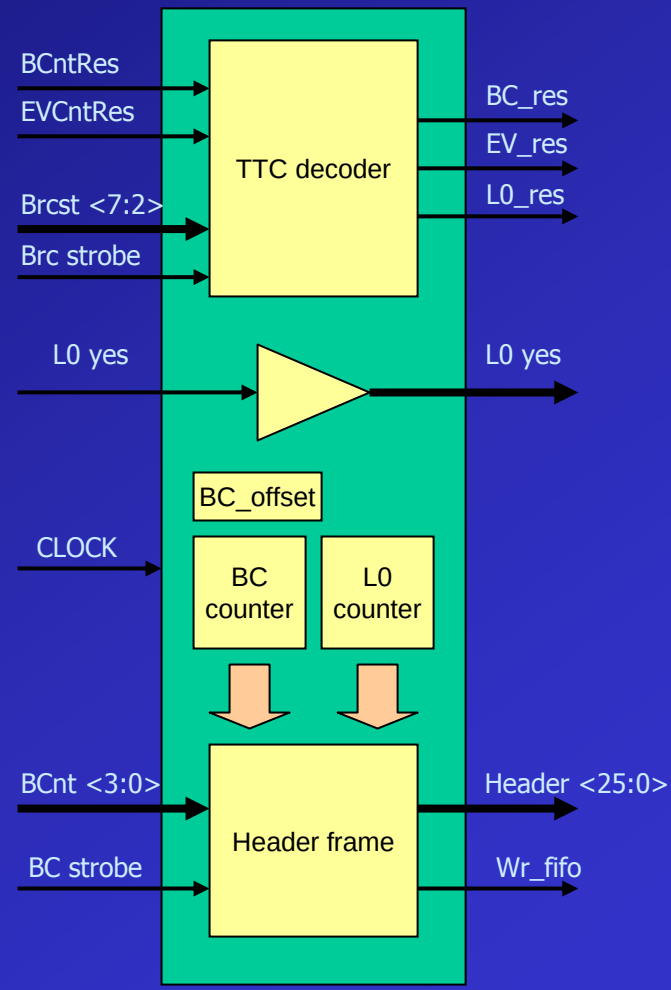
GOL interconnection



Paolo Ciambrone INFN- LNF

TTC decode

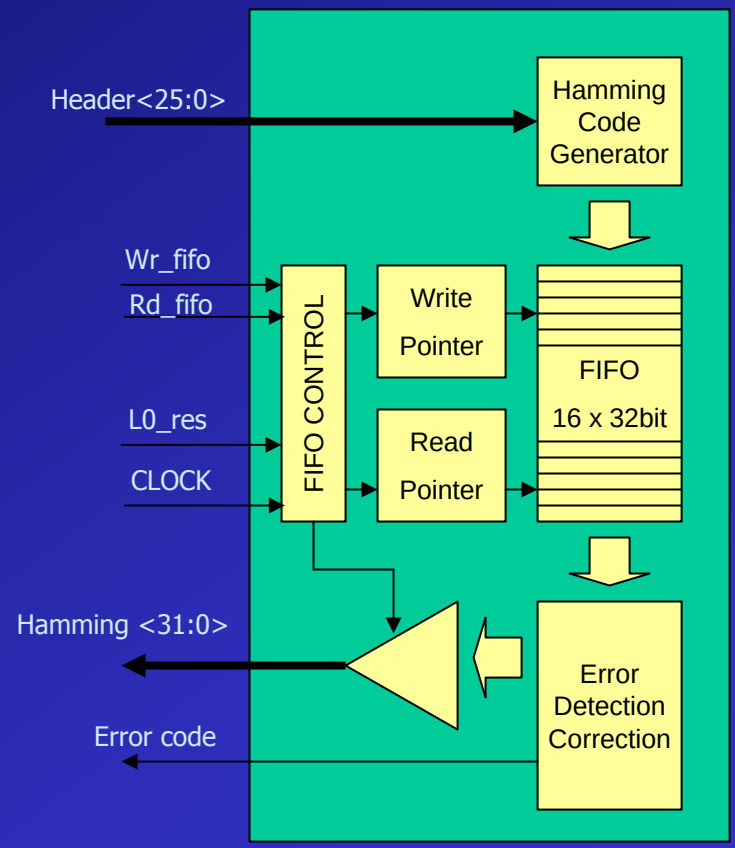
- Receive signals from TTCrx
  - Decode broadcast command
    - Bunch-ID reset (BC_res)
    - L0 Event ID reset (EV_res)
    - L0 reset (L0_res)
  - Distribute resets and L0 trigger signals
- Internal 12 bit Bunch-ID counter (BC_Id)
  - Synchronous reset with BC_res
  - Predefined BC_offset loaded at BC_res
- Internal 12 bit L0 Event-ID counter (L0_Id)
  - Synchronous reset with EV_res or L0_res
  - First L0 trigger after a counter reset ⇒ L0_Id=0
- For each L0 trigger
  - Check internal BC_Id *vs* TTCrx BCnt
  - Generate header word (25 bit)
    - 1 check bit + 12 bit L0_Id + 12 bit BC_Id
  - Generate header FIFO write



Paolo Ciambrone INFN- LNF

FIFO header

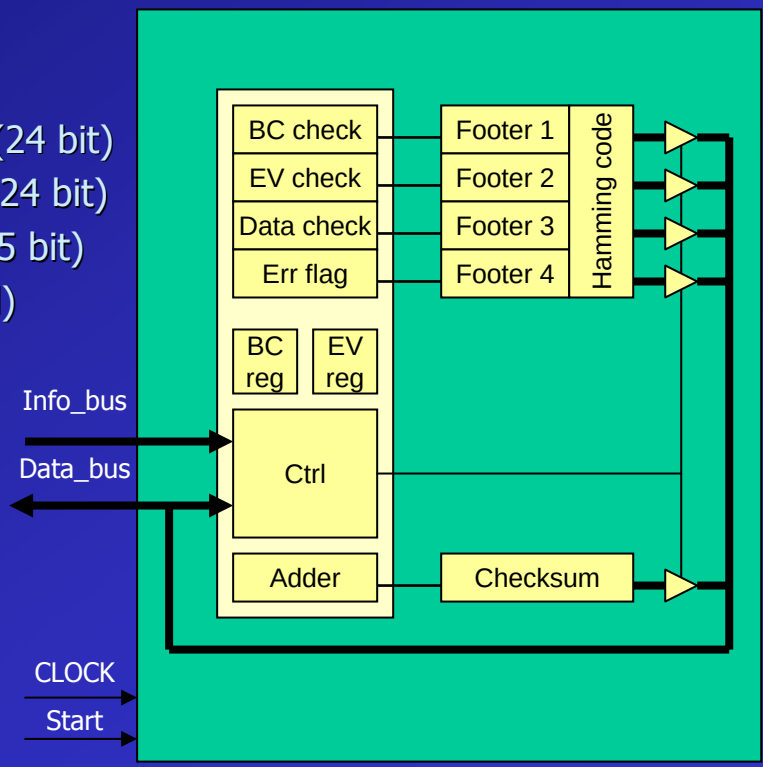
- Allow consecutive L0 trigger
  - 16 words deep
  - 32/64 in final version (?)
- Data protected by Hamming code
  - Single error detection and correction
  - Double error detection
  - 6 extra code bit
- Data discharged at FIFO full
- FIFO reset with L0_res



Paolo Ciambrone INFN- LNF

CHK footer

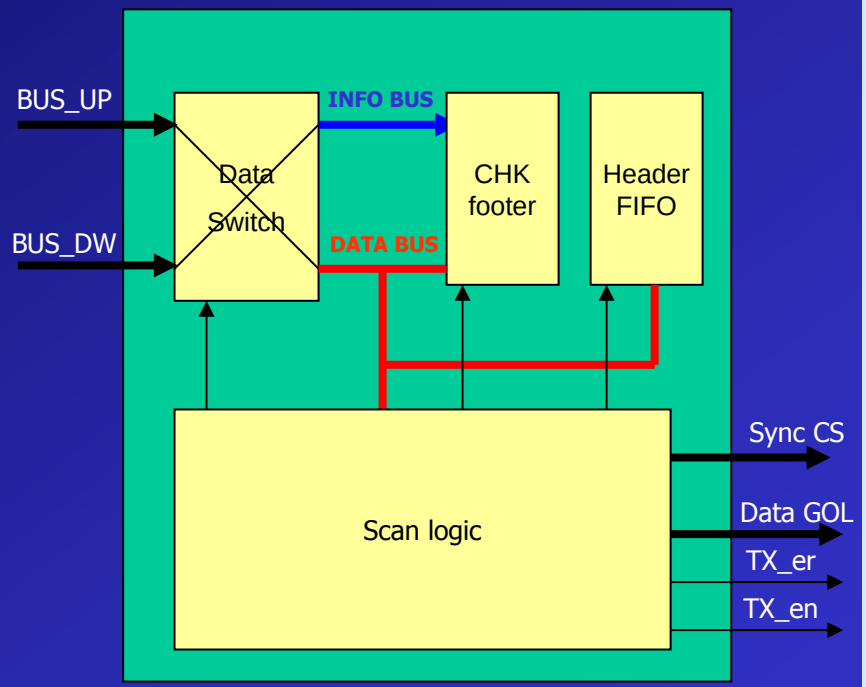
- Receive INFO word
  - 4 bit SYNC BX_Id
  - 4 bit SYNC EV_Id
  - 2 bit SYNC data error (double error detection)
- Generate 4 footer check words
  - BX_Id alignment of each SYNC *vs* internal BC_Id (24 bit)
  - EV_Id alignment of each SYNC *vs* internal L0_Id (24 bit)
  - Data error of each SYNC + internal FIFO error (25 bit)
  - Board address + Error flags (not yet implemented)
- Footer protected by Hamming code
- Calculate frame checksum
  - 32 bit adder without carry
    - Header
    - 24 data words
    - 4 footer check words

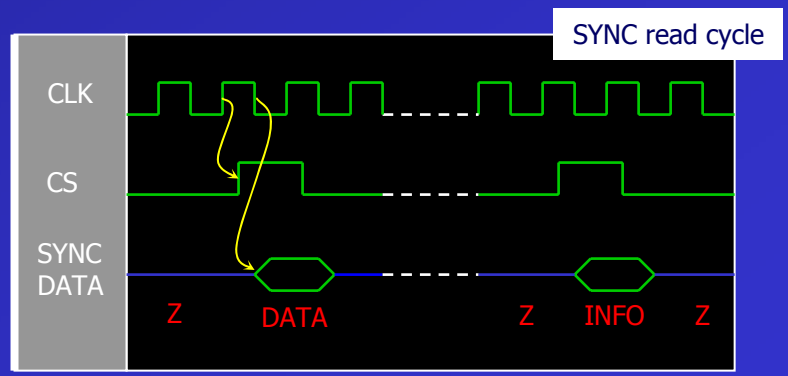


Paolo Ciambrone INFN- LNF

Scan logic

- Scan start if header FIFO is not empty
- Drive GOL transmission
- Read header FIFO
  - Store BC_Id and L0_Id in internal registers
  - Send hamming header to GOL
- Read SYNC chip in parallel mode
  - Drive dataswitch to redirect BUS_UP and BUS_DW on internal buses
  - For the first 12 clock cycles
    - Receive data word on BUS_UP
    - Receive info word on BUS_DW
  - For the second 12 clock cycles
    - Receive data word on BUS_DW
    - Receive info word on BUS_UP
  - Send data words to GOL with 1-level pipeline
- Read and send footer check words and checksum to GOL

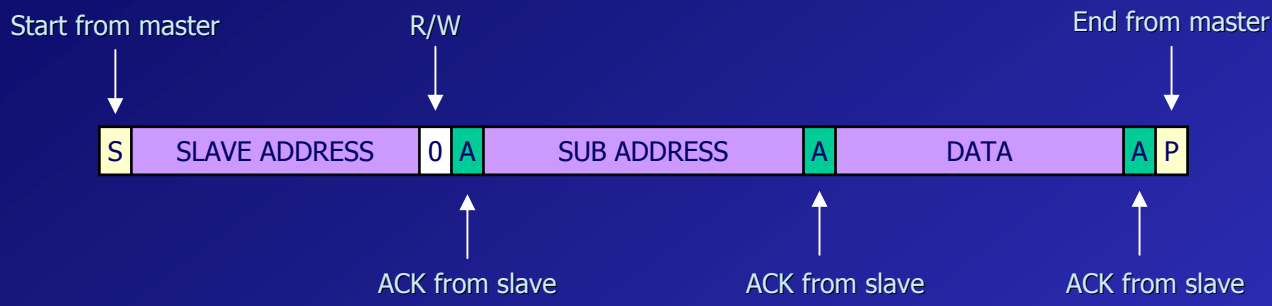




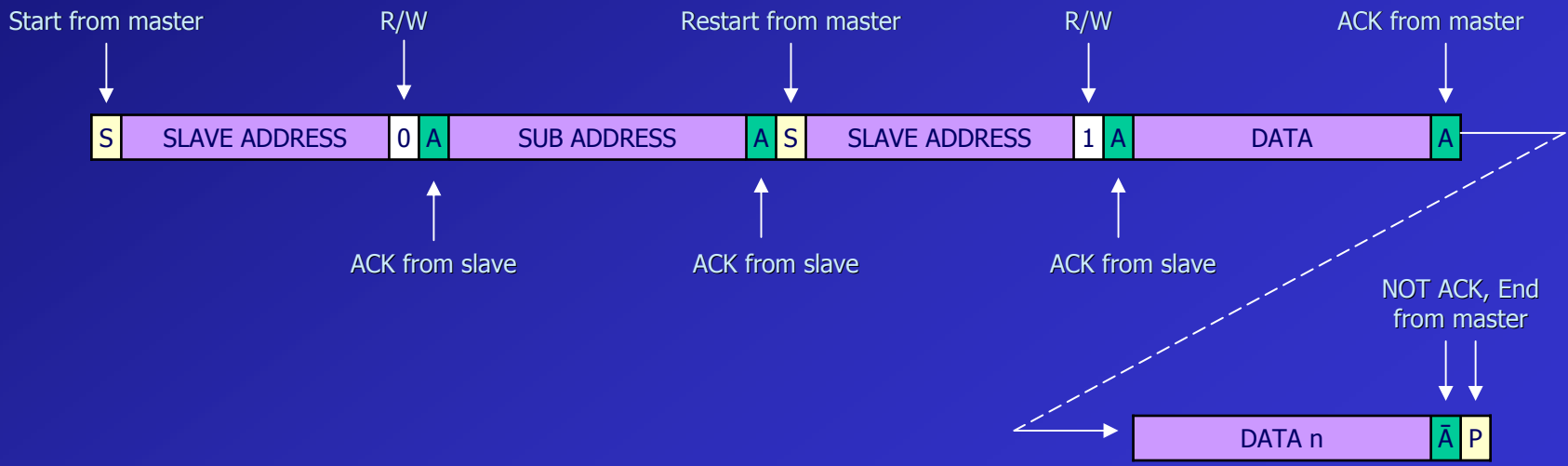
Paolo Ciambrone INFN- LNF

I²C interface

- I²C interface implemented on L0 controller
  - Write cycle



  - Read cycle



Paolo Ciambrone INFN- LNF