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**LHCb Experiment**

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**Boards IMB**

Description: **Boards IMB**

Eq. Code: EDMS Id: **LHCb-0315 v.0**

Responsible:

Documents in this node: 3 [Create Doc.](#) [Advanced](#)

**609484 v.1** Intermediate Board **In Work**

EDMS Id 609484

The Intermediate Boards merge 26680 front-end channels to generate 9408 logical channels

[Doc. page](#) IB\_sch pdf (1 Mb) 0 sub-doc 1 version [Giulietto FELICITO](#) 2005-07-11 Specification

IB\_pcb pdf (205 kb)

IB\_CADENCE\_archive zip (5 Mb)

**610067 v.1** IB\_PRR **In Work**

EDMS Id 610067

Intermediate Board system ppt

[Doc. page](#) IB\_Document doc (4 Mb) pdf (3 Mb) 0 sub-doc 1 version [Giulietto FELICITO](#) 2005-07-12 Specification

IB\_System ppt (12 Mb) pdf (6 Mb)

**615687 v.1** Transition Board **In Work**

EDMS Id 615687

The board used to match low density front-end connector modularity with the Intermediate Board high density connector

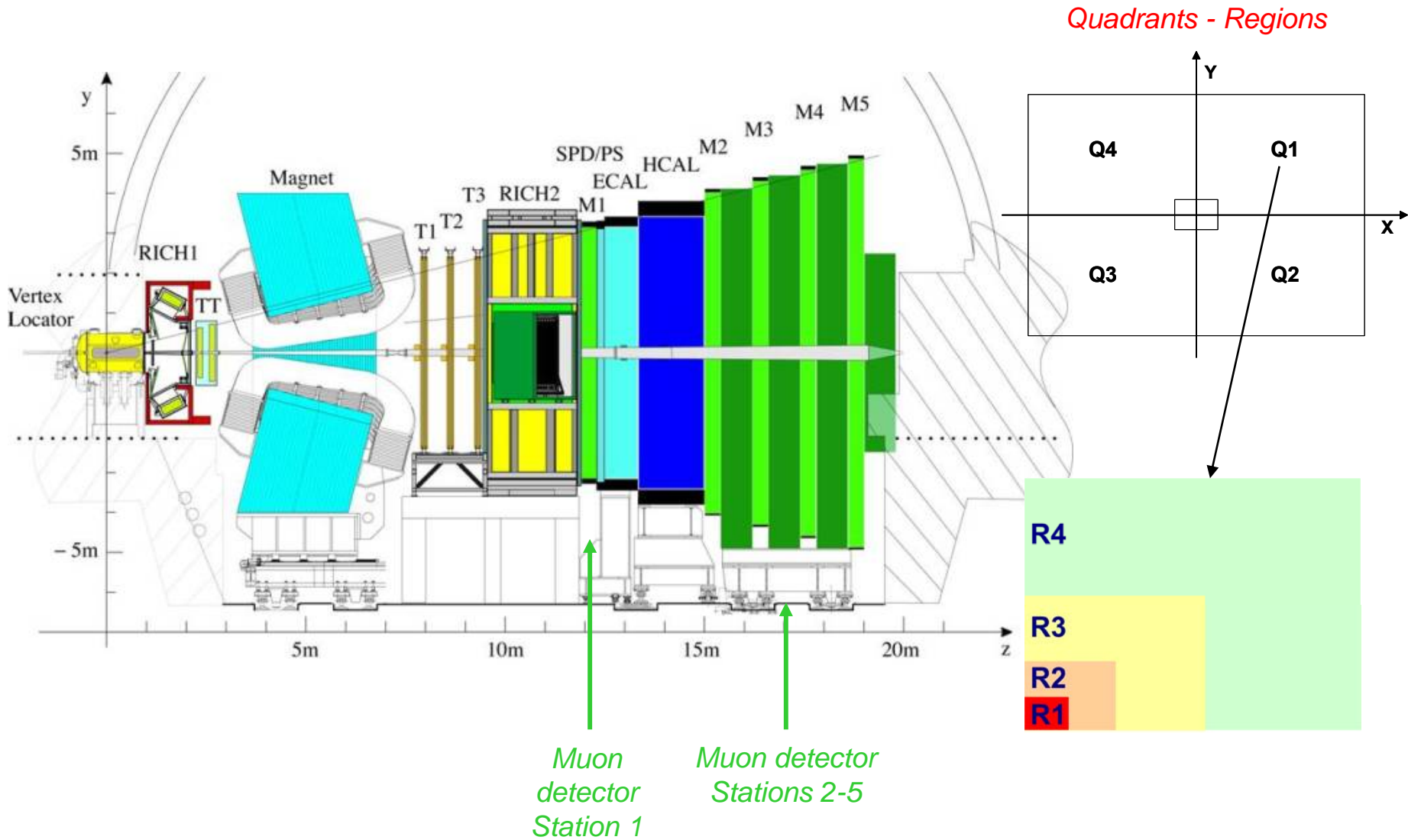
[Doc. page](#) TB\_sch pdf (550 kb) 0 sub-doc 1 version [Giulietto FELICITO](#) 2005-07-14 Specification

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**PRR – IB System**

Intranet locale

- Why do we need the IB System ?
  - The apparatus
  - FEE Channels & Logical Channels
  - The FE chain
  - Station and Regions
  
- The IB System architecture
  - The IB and the TB boards
  - The IB and TB crate
  
- System qualification
  - Skew requirements
  - Skew measurements
  - Prototypes qualification test setup
  - Skew measurement results
  - Mass production test setup
  - Irradiation Test
  - Conclusions
  - Detector mapping example



**FEE channels**



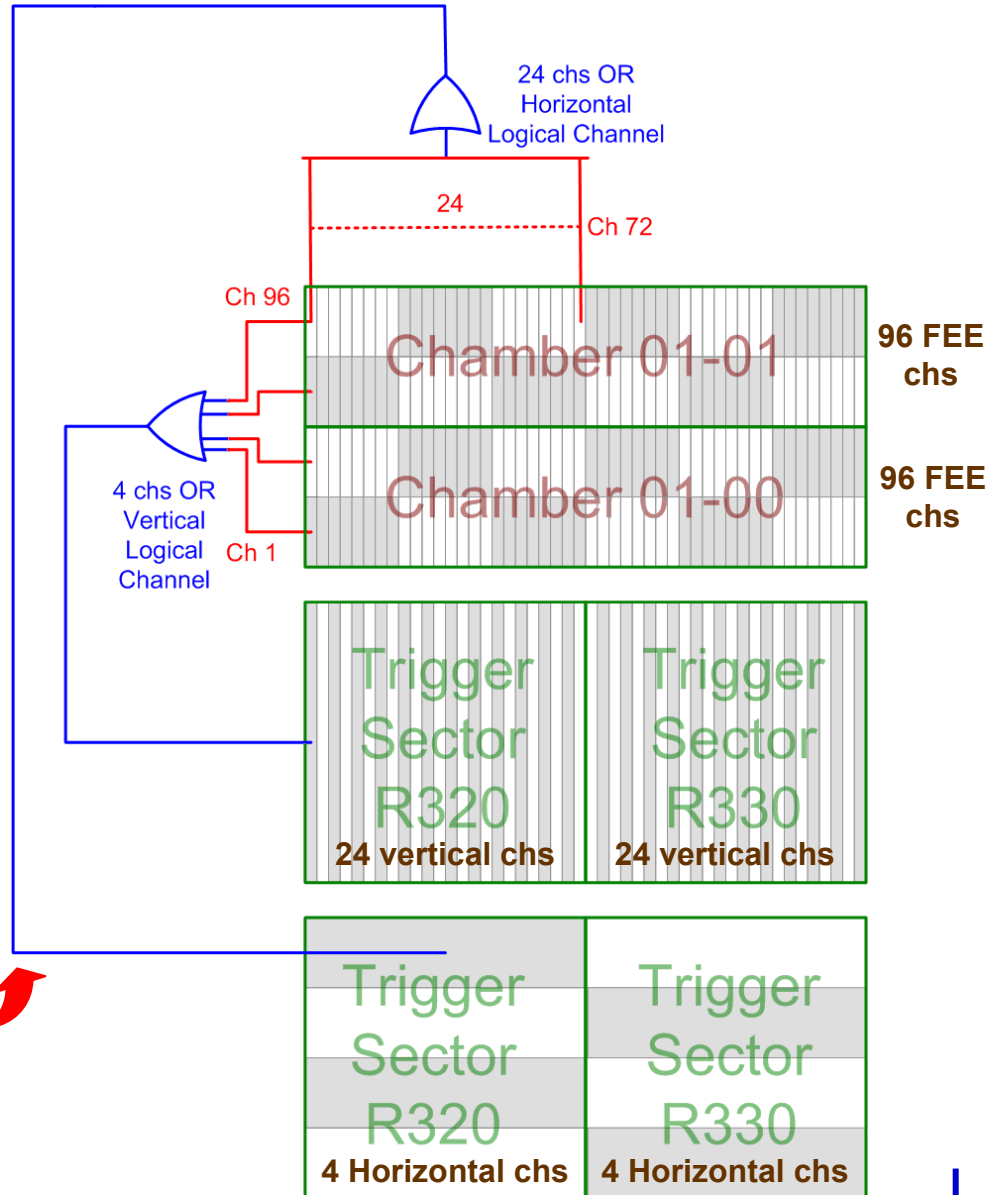
**Logical channels**



**Trigger Sectors**

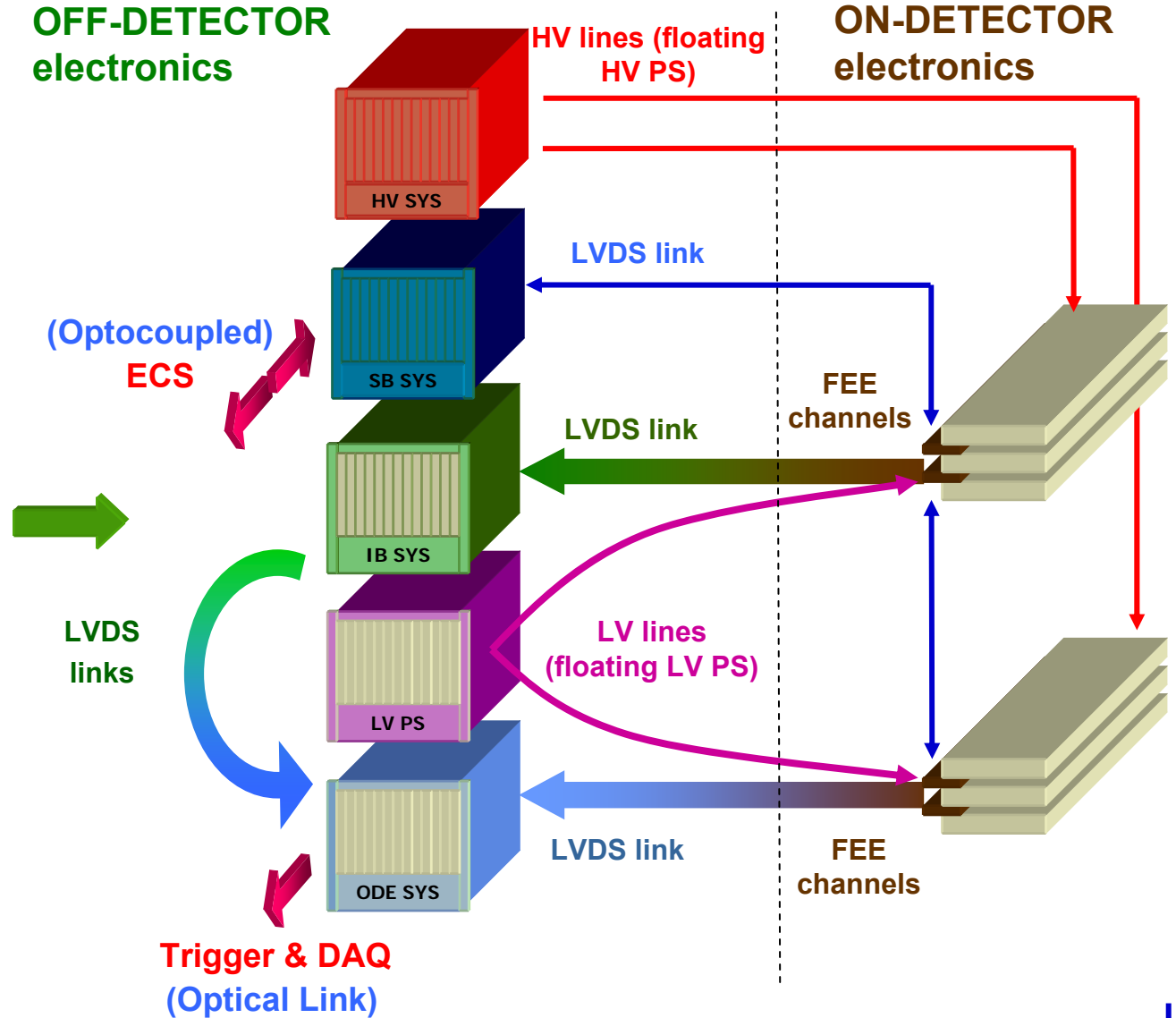
*Because of single channel occupancy and electrode capacitance the detector segmentation for trigger propose is coarser than the physical one*

**An example : M2/M3 R3**



The IB System is used to merge 26880 FE channels and to generate 9408 logical channels

Five different configurations are required to readout the muon detector

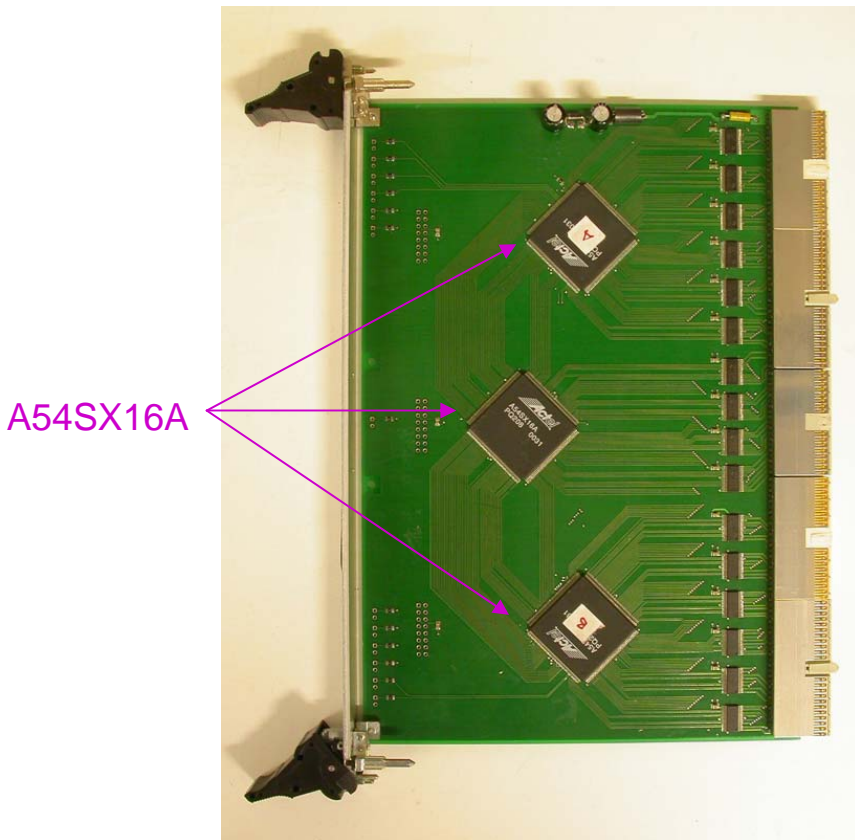


Station	Region	Number of optical links per quarter of region	Number of pads per optical links	Number of horizontal strips per optical link	Number of vertical strips per optical link	Total number of logical channels per link
M1	R1	24	24			24
	R2					
	R3					
	R4					
M2 or M3	R1	12		16	12	28
	R2	24		4	12	16
	R3	12		4	24	28
	R4	12		4	24	28
M4 or M5	R1	12	24			24
	R2	12		8	6	14
	R3	12		4	6	10
	R4	12		4	6	10

Six TS configurations  Six IB types

Single PCB  
Six FPGA configurations

Single Transition Board  
Six input cable configurations



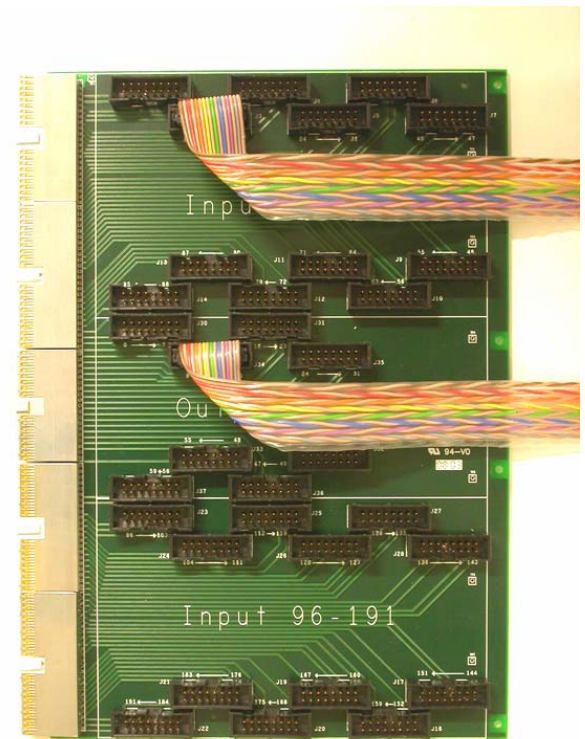
Up to 96  
LVDS chs in



Up to 64  
LVDS chs out

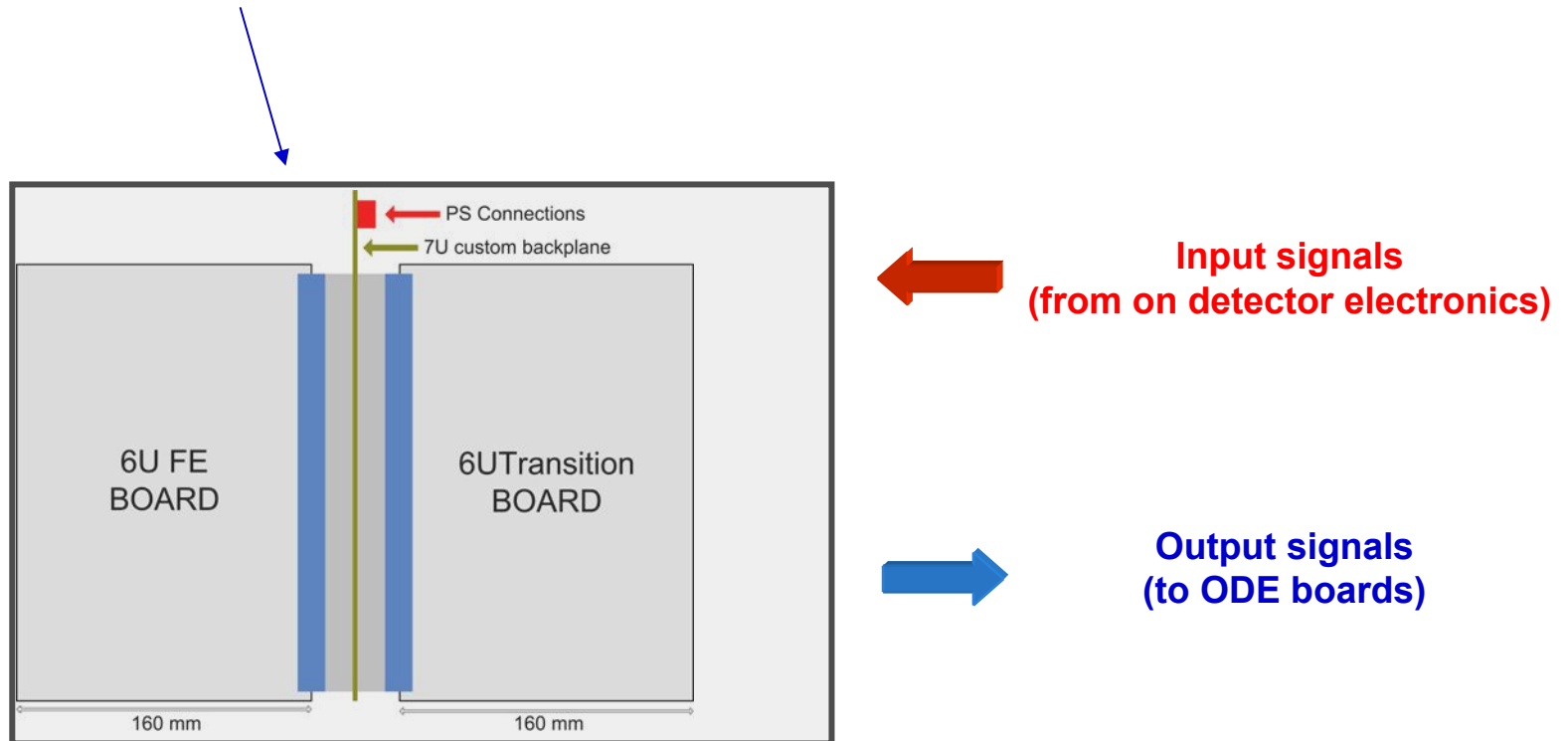


Up to 96  
LVDS chs in





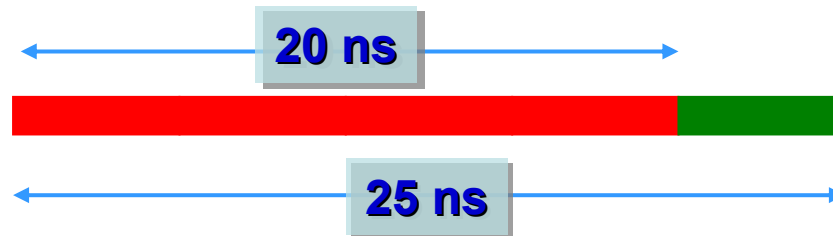
## 7U crate instrumented with custom backplane



- simplifies maintenance (IB can be easily replaced in case of failure)
- simplifies cabling



skew between logical output channels must be minimized as much as possible to maximize efficiency

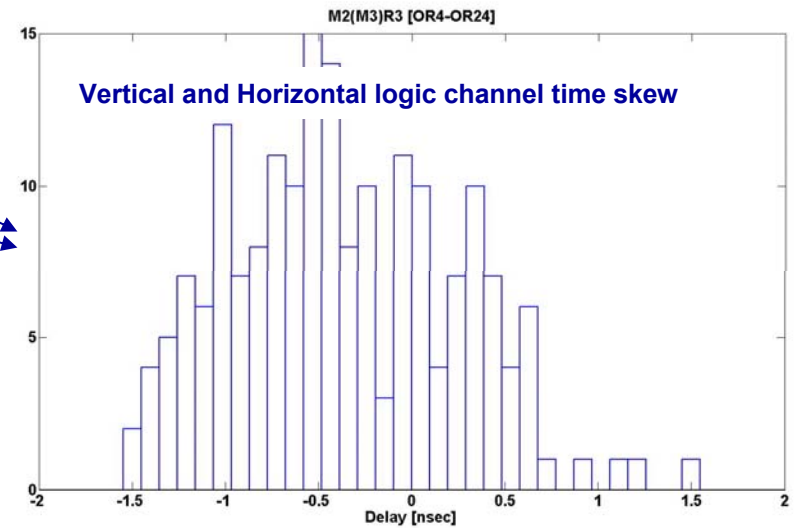
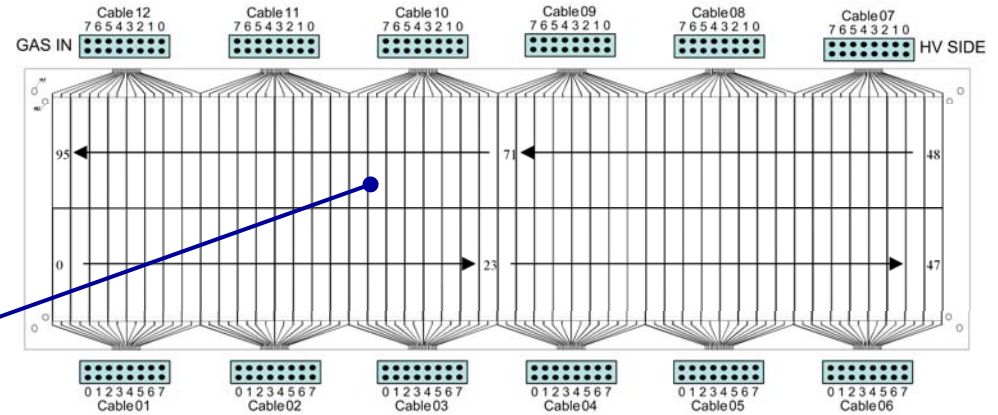
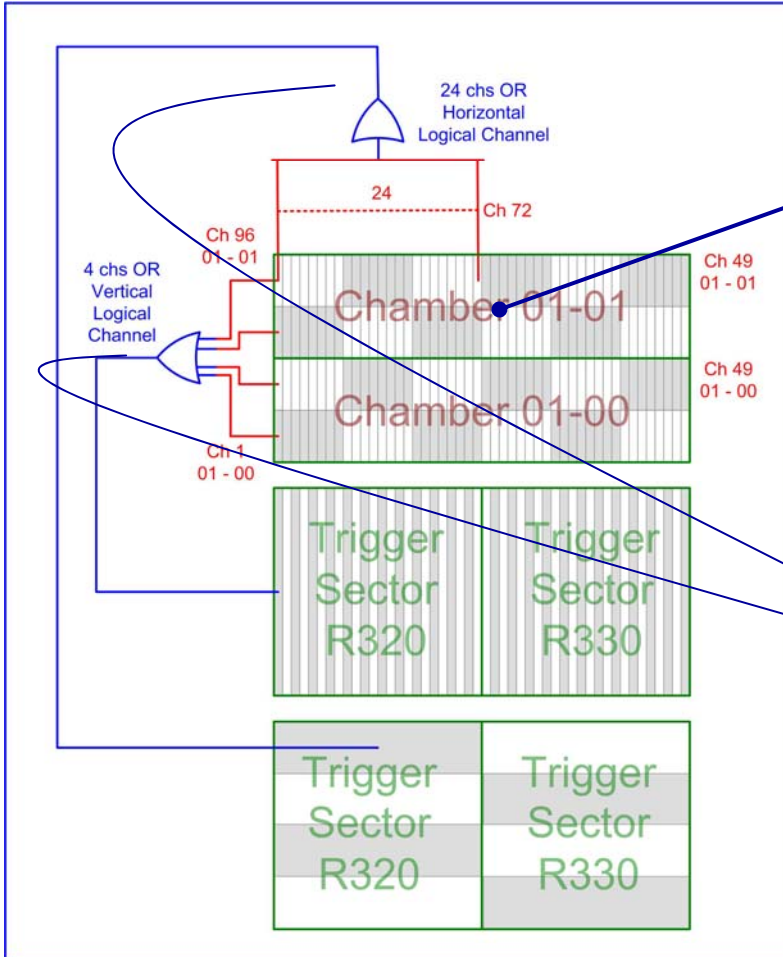


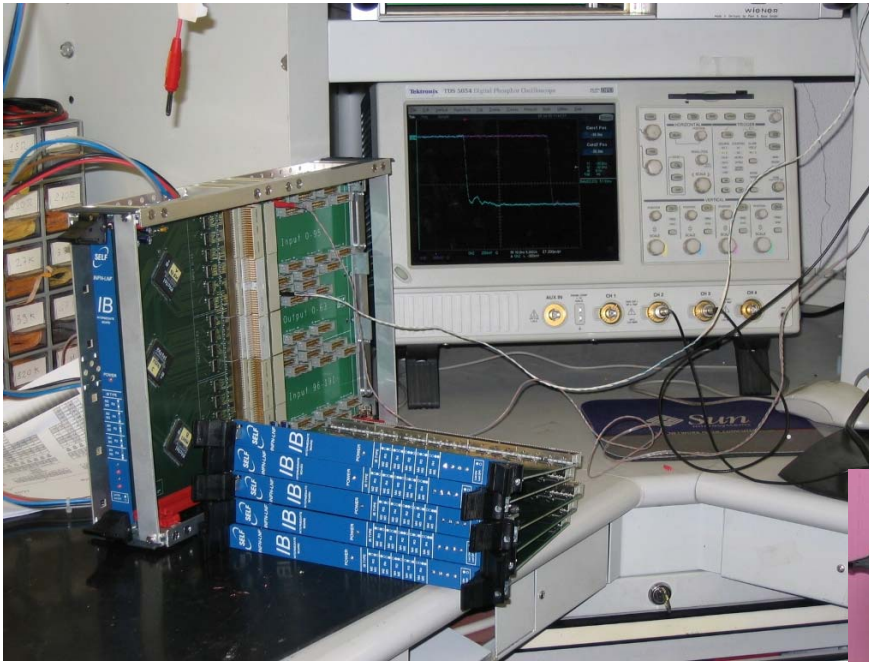
Front-End single channel delay adjustment capability : ~ 1.6 ns step (50 ns)



**The electronics and cables contribution to jitter and skew must be less than 3 ns**

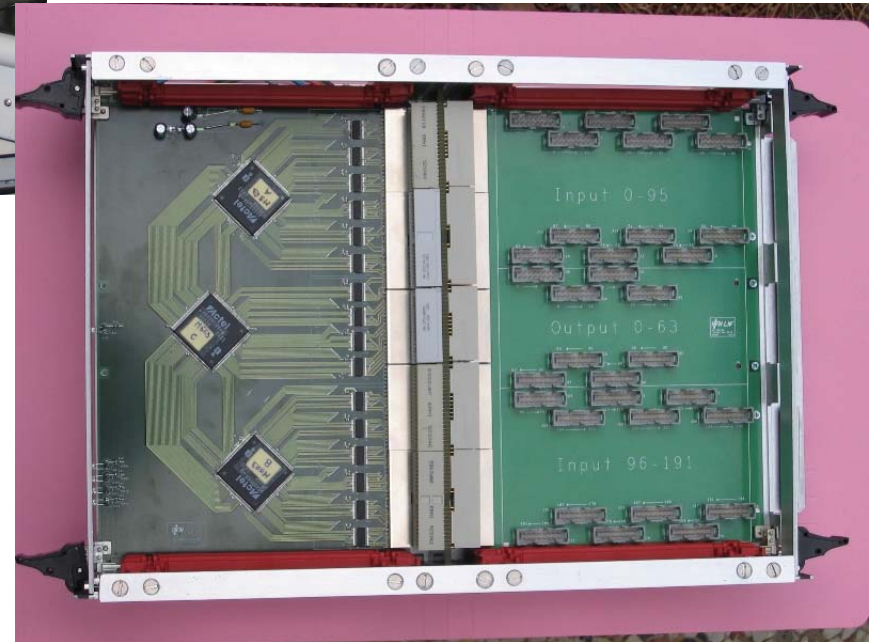
## An example M3R3

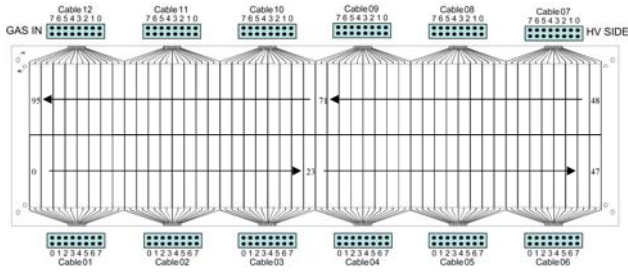
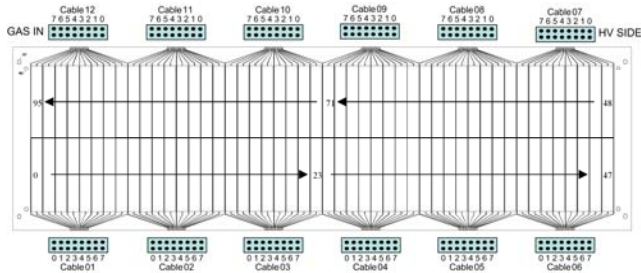




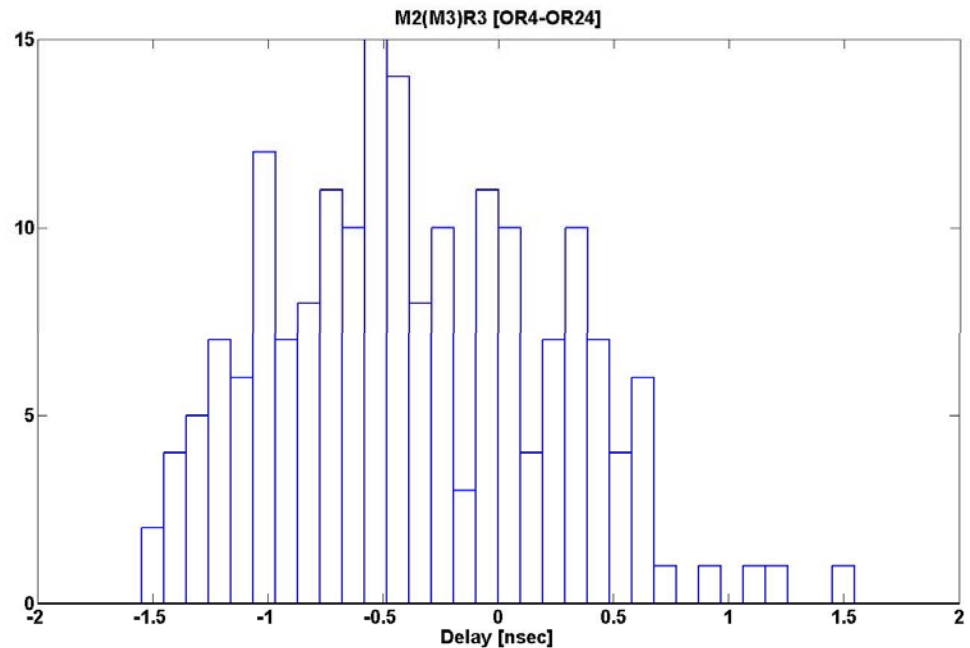
IB setup measurements  
for skew measurements  
(prototypes qualification)

Mini-crate for IB & TB test





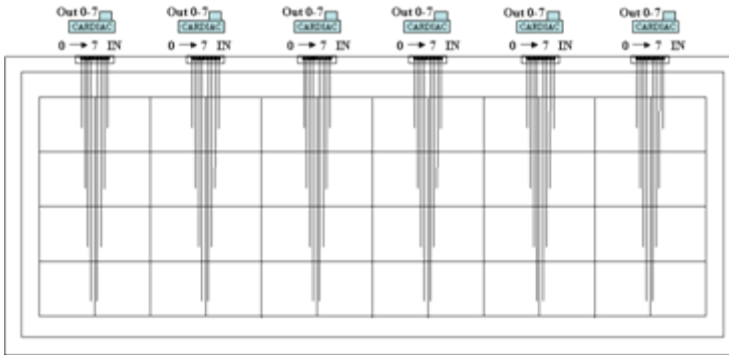
## M2(M3)R3



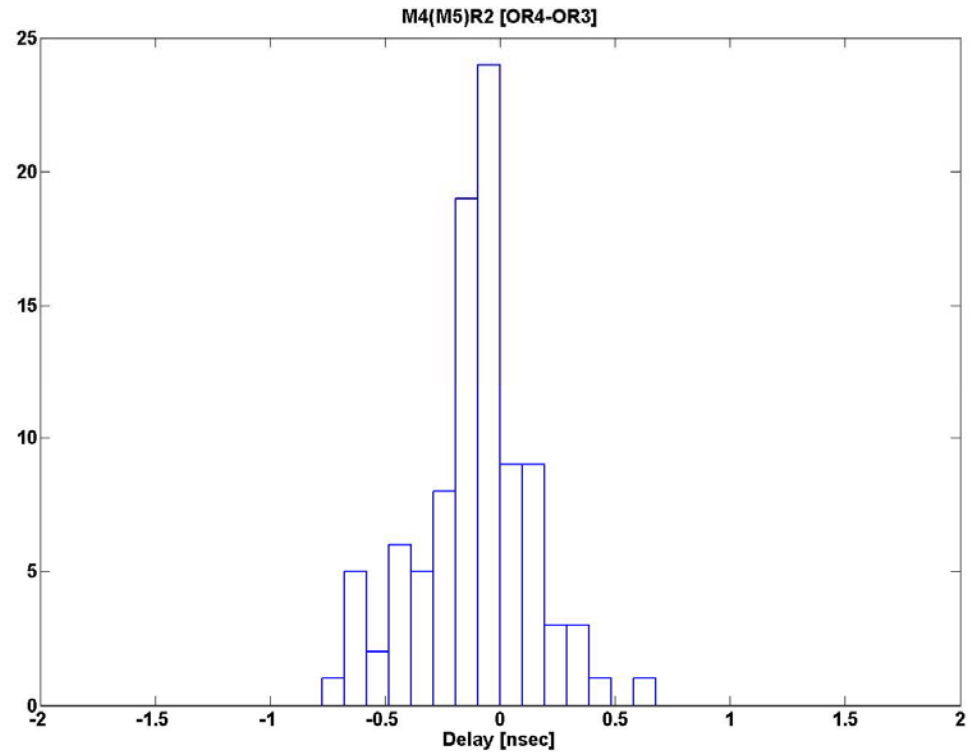
Trigger Sector → 24 Vertical strips + 4 horizontal strips



## M4(M5)R2

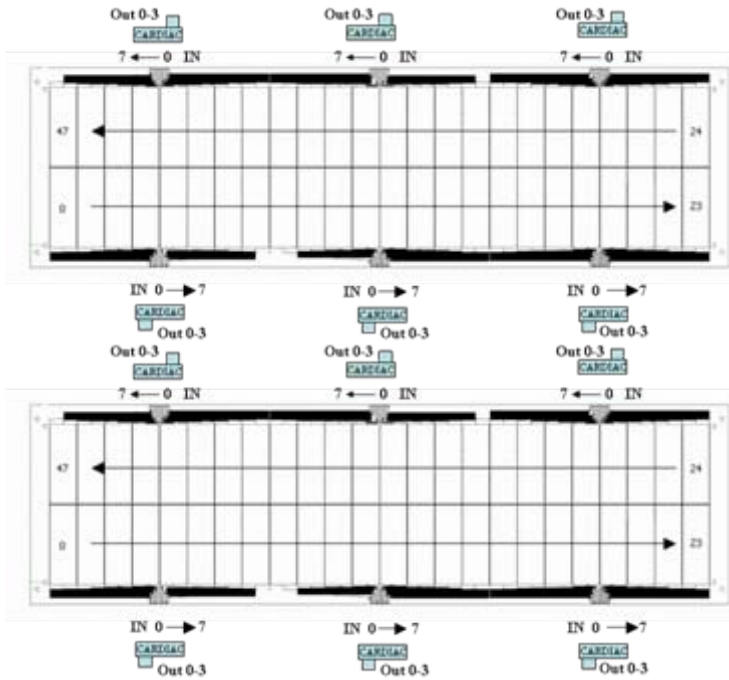


0	7	8	15	16	23	24	31	32	39	40	47
1	6	9	14	17	22	25	30	33	38	41	46
2	5	10	13	18	21	26	29	34	37	42	45
3	4	11	12	19	20	27	28	35	36	43	44



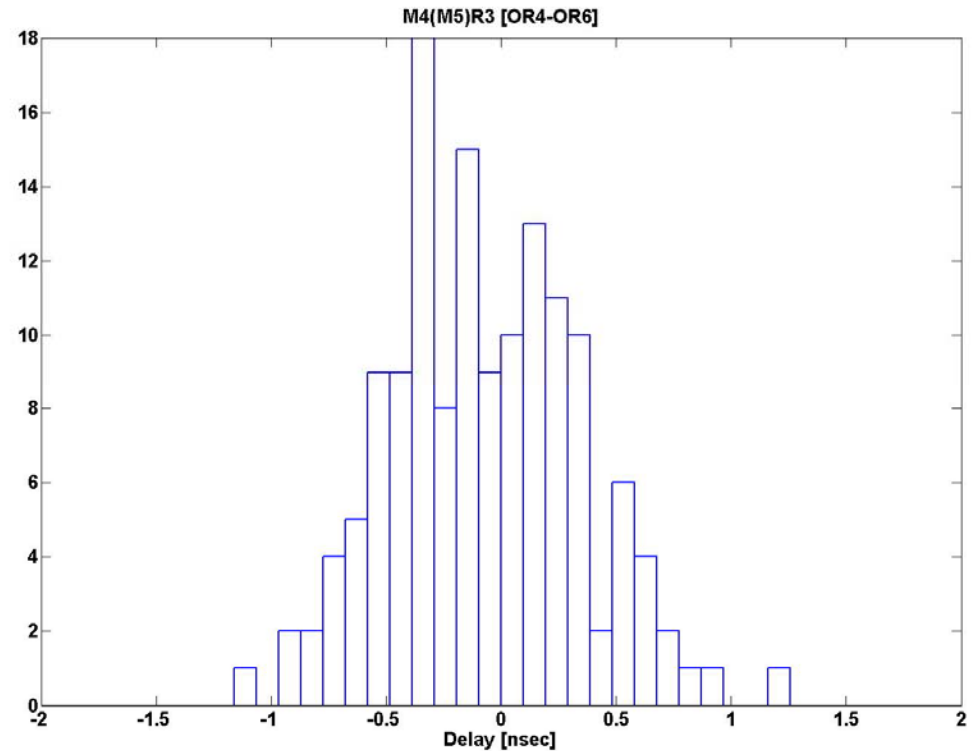
Trigger Sector → 6 Vertical strips + 8 horizontal strips





23	22	21	20	19	18	17	16	15	14	13	12
0	1	2	3	4	5	6	7	8	9	10	11
23	22	21	20	19	18	17	16	15	14	13	12
0	1	2	3	4	5	6	7	8	9	10	11

## M4(M5)R3



Trigger Sector → 6 Vertical strips + 4 horizontal strips

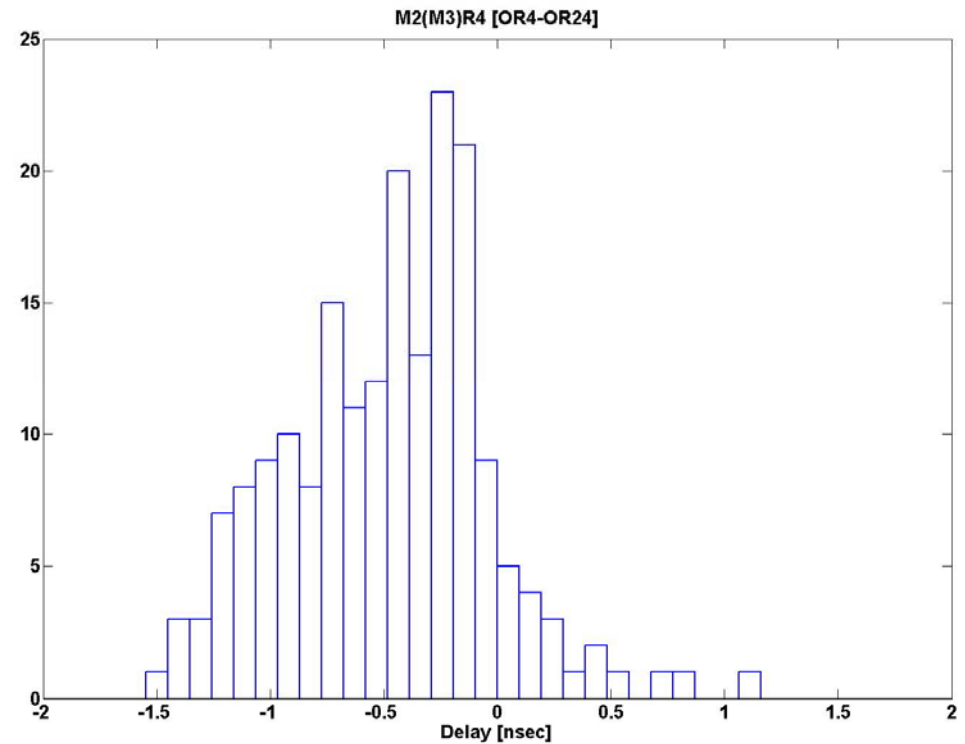


## M4(M5)R4



R402

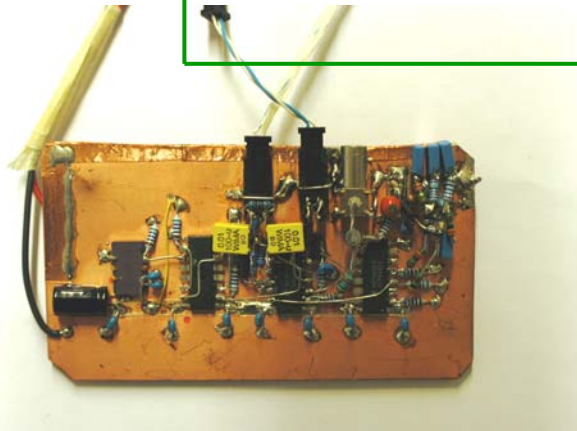
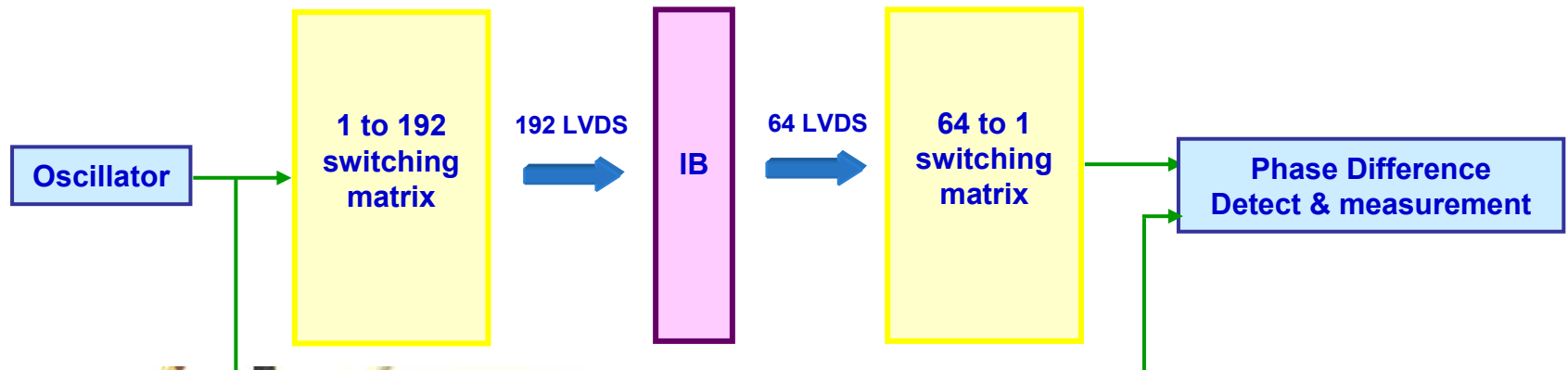
1	2	3	4	5	6
1	2	3	4	5	6
1	2	3	4	5	6
1	2	3	4	5	6



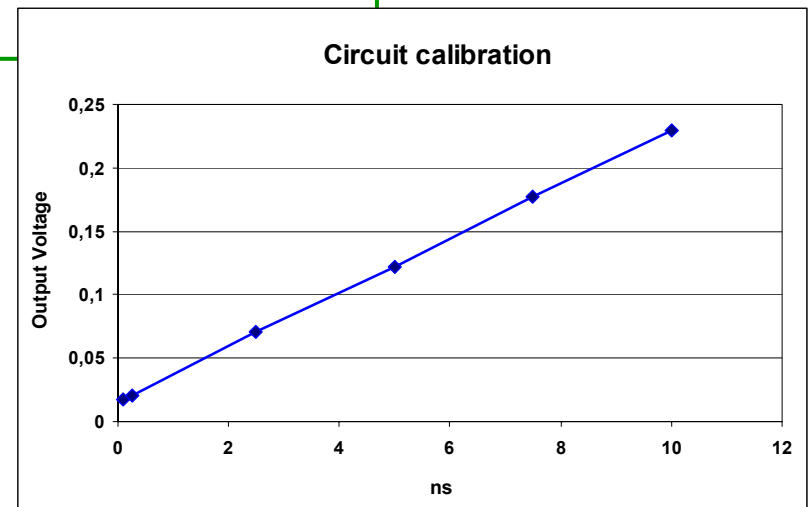
Trigger Sector → 6 Vertical strips + 4 horizontal strips

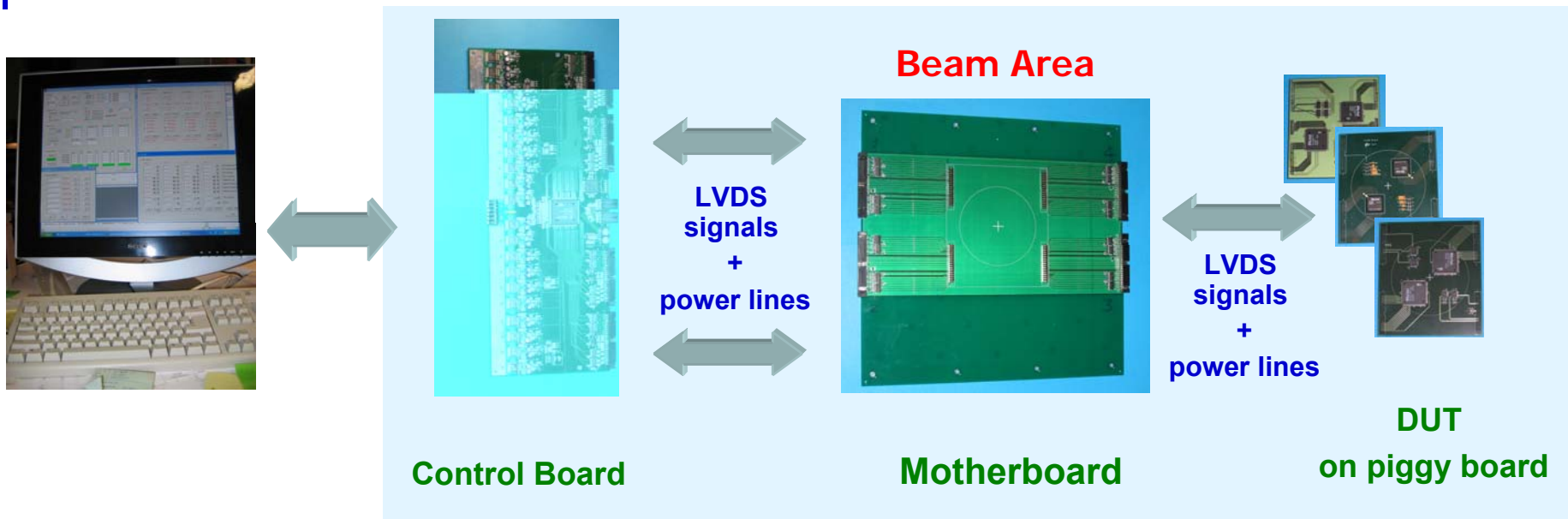
A measurement system has been developed for IB production test. The system features:

- a switching matrix for input/output delay measurement (192 differential inputs / 64 differential outputs)
- a new measurement method based on input/output signal phase measurement



Delay measurement circuit prototype





## Proton beam at Louvain la Neuve Cyclotron

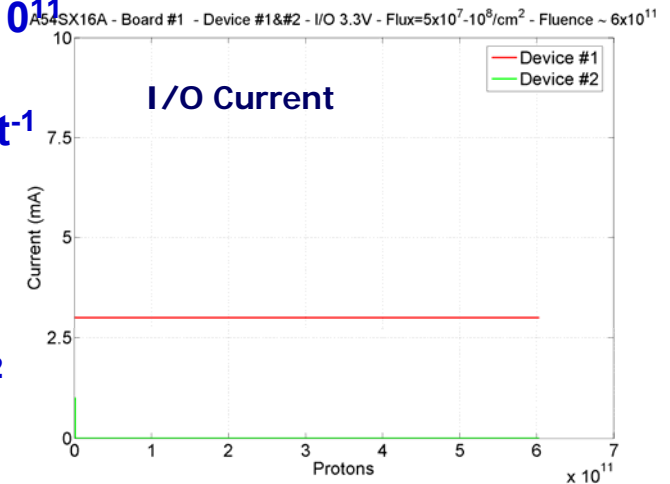
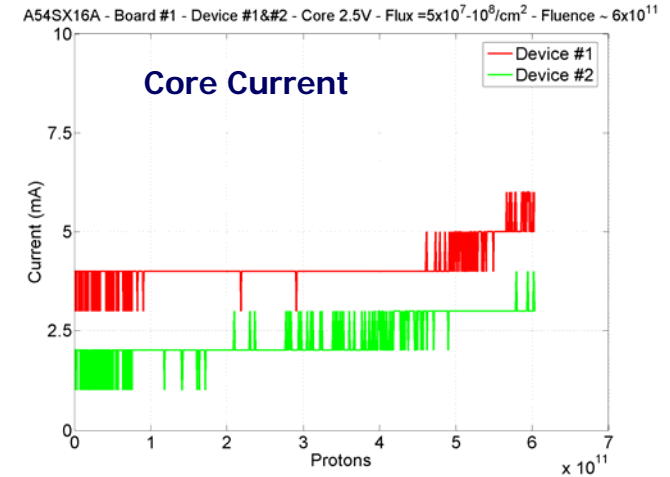
- Energy: ~ 70 MeV
- Nominal flux used
  - $5 \times 10^7$  protons  $\text{cm}^{-2} \text{s}^{-1}$  up to  $10^{11}$  protons  $\text{cm}^{-2}$
  - $5 \times 10^8$  protons  $\text{cm}^{-2} \text{s}^{-1}$  up to  $6 \times 10^{11}$  protons  $\text{cm}^{-2}$
- Fluence of  $6 \times 10^{11}$  protons  $\text{cm}^{-2}$  correspond to:
  - $\sim 6 \times 10^{11}$  “energetic” hadrons ( $\sim 120$  years of LHCb muon life)
  - $\sim 68.5$  krad of TID ( $\sim 86$  years of LHCb muon life)
  - $\sim 9 \times 10^{11}$  neutrons  $\text{cm}^{-2}$  for NIEL ( $\sim 10$  years of LHCb muon life)

### A54SX16A

- **Anti-fuse** based FPGA
- **0.22μm/0.25μm CMOS Process Technology**
- **24000 (16000) system gates (typical gates)**
- **924 combinatorial cells**
- **528(990) dedicated flip-flops (maximum flip-flops)**

### Irradiation results

- **No SEU observed in flip-flops up to a fluence of  $6 \times 10^{11}$  protons/cm<sup>2</sup>**
  - **Cross section per bit  $< 2.1 \times 10^{-14}$  cm<sup>2</sup> protons<sup>-1</sup> bit<sup>-1</sup>**
- **No clock or control logic upset observed**
- **No SEL detected**
- **No change in I/O current @  $6 \times 10^{11}$  protons/cm<sup>2</sup>**
- **Small changes in Core current @  $6 \times 10^{11}$  protons/cm<sup>2</sup>**



## LVDS Drivers : SN75LVDS289

- No SEU observed in flip-flops up to a fluence of  $6 \times 10^{11}$  protons/cm<sup>2</sup>
- No SEL detected
- No change in current @  $6 \times 10^{11}$  protons/cm<sup>2</sup>

## LVDS Receivers : SN75LVDT288

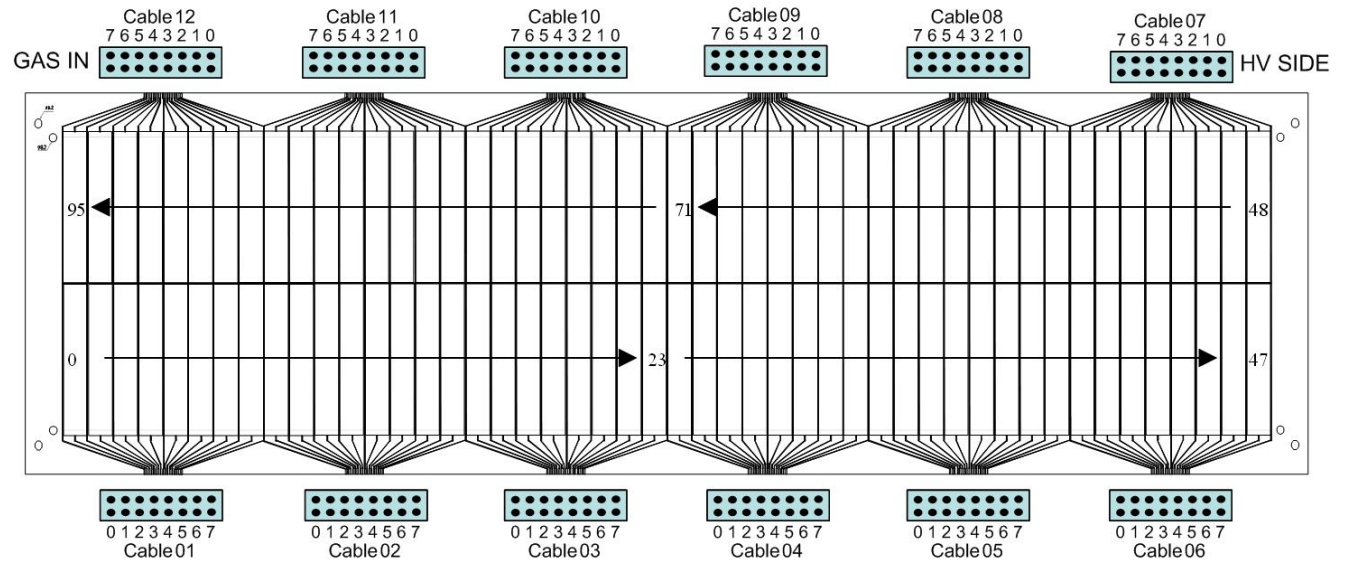
- No SEU observed in flip-flops up to a fluence of  $6 \times 10^{11}$  protons/cm<sup>2</sup>
- No SEL detected
- No change in current @  $6 \times 10^{11}$  protons/cm<sup>2</sup>

- ✓ The Intermediate Board system is used to match FEE granularity and Trigger logic requirements
- ✓ 6 different logic configurations are required to match the whole muon detector
- ✓ A single (halogen free) PCB board together with anti-fuse programmable logic has been used to implement the configurations.
- ✓ Six prototypes corresponding to the six required configurations have been produced and tested
- ✓ Skew measurements are within the design specs
- ✓ FPGA/Drivers/Receivers do not show any problem up to a fluence of  $6 \times 10^{11}$  protons/cm<sup>2</sup>
- ✓ A test setup for IB mass production has been designed. The circuit features an input-output switching matrix allowing single channel delay measurement with a resolution less than 100 ps

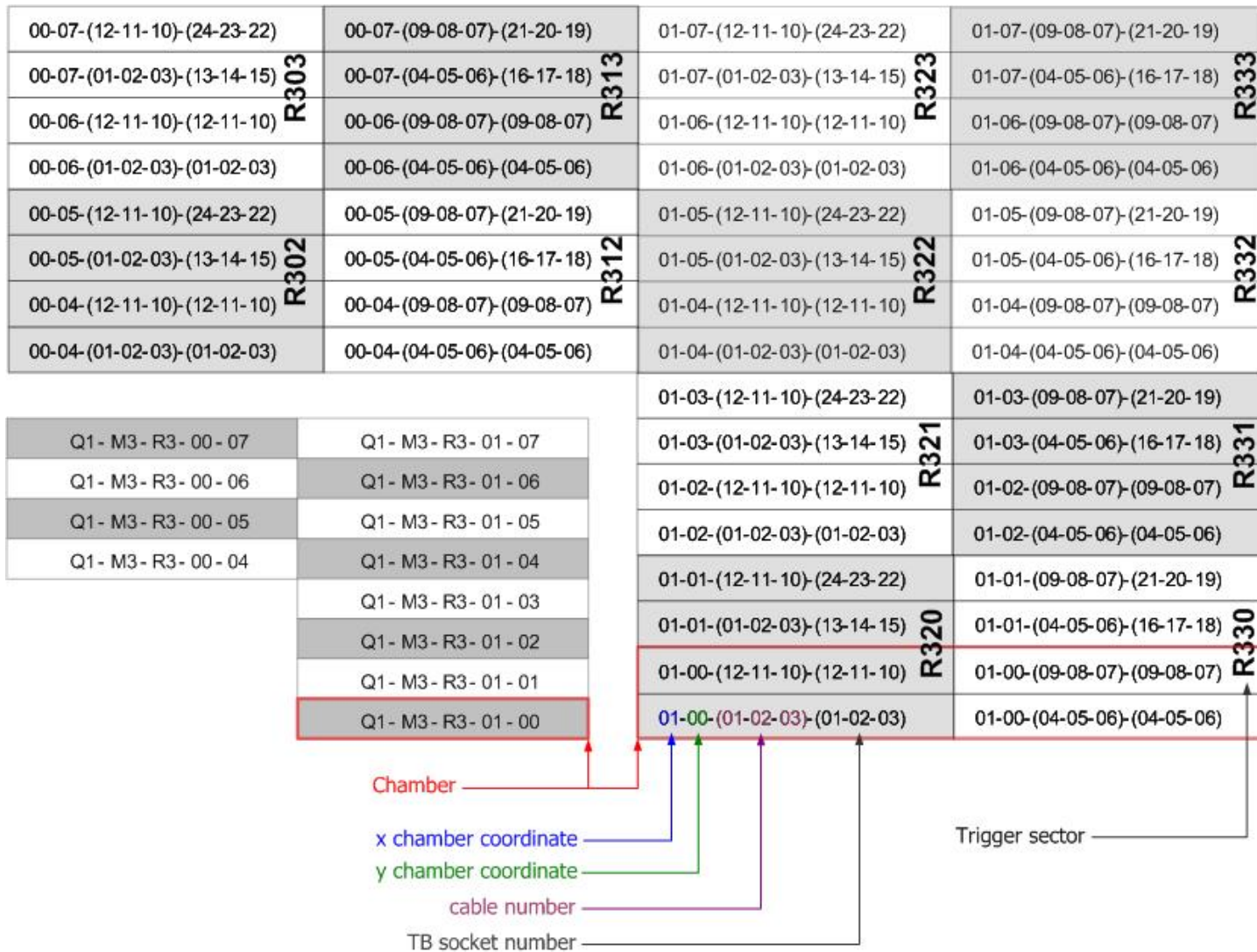
To design both the Transition Board and the Intermediate Boards the detector signal full path must be considered ...

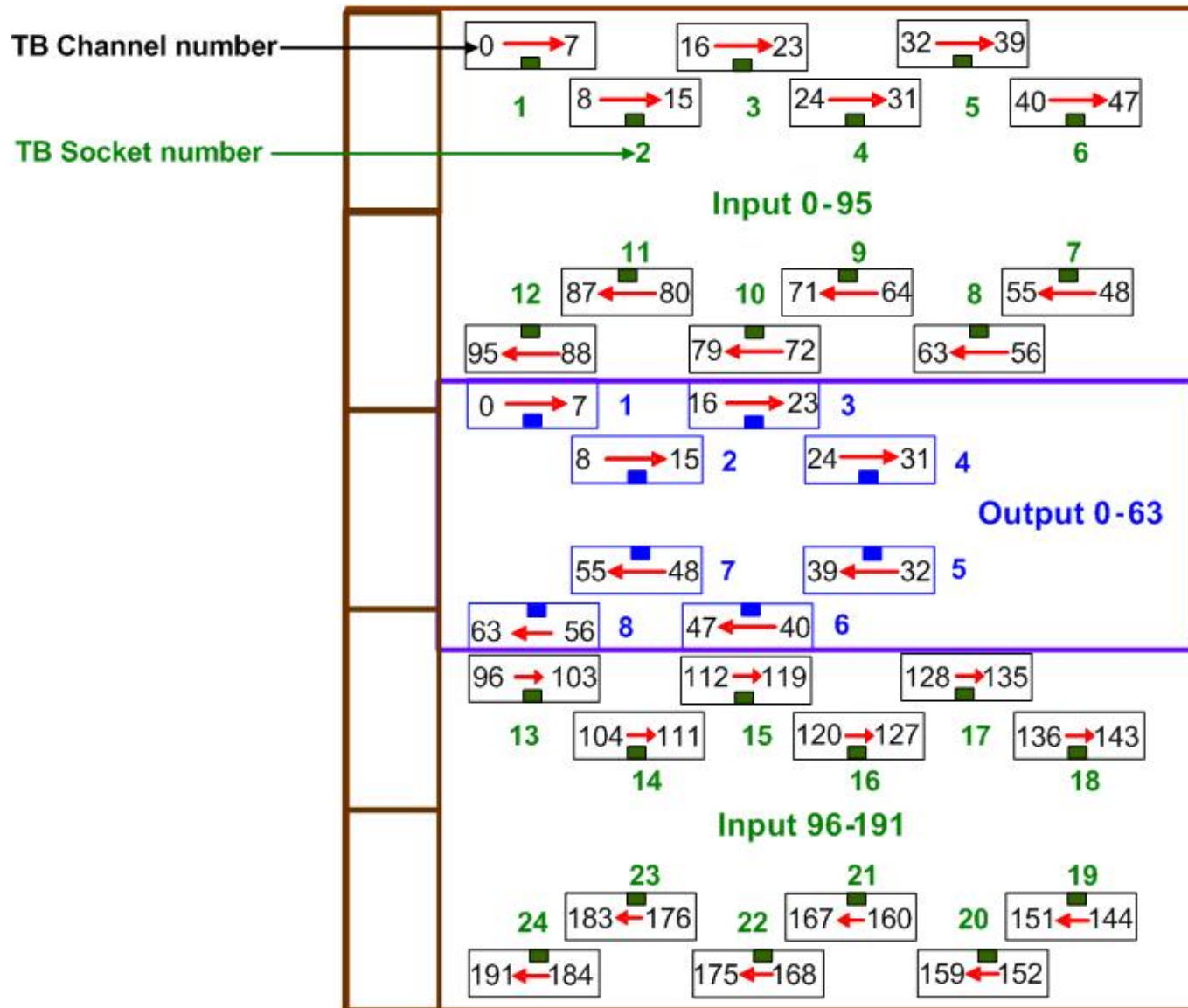
➔ The muon detector mapping for M2R2, M2(M3)R3-R4, M4(M5)R2-R3-R4 comes for free ➔

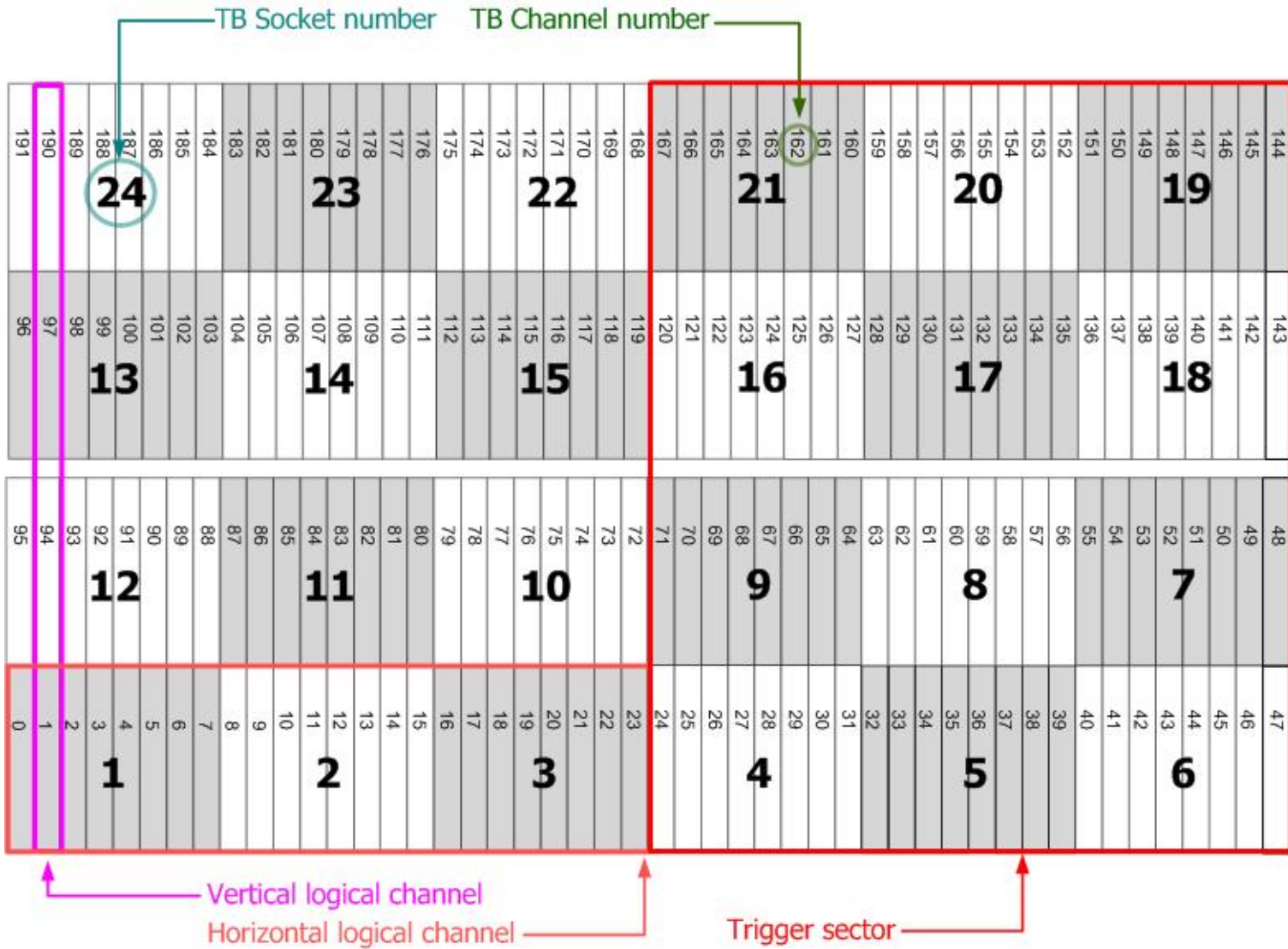
Mapping example  
➔ M3(M4)R3

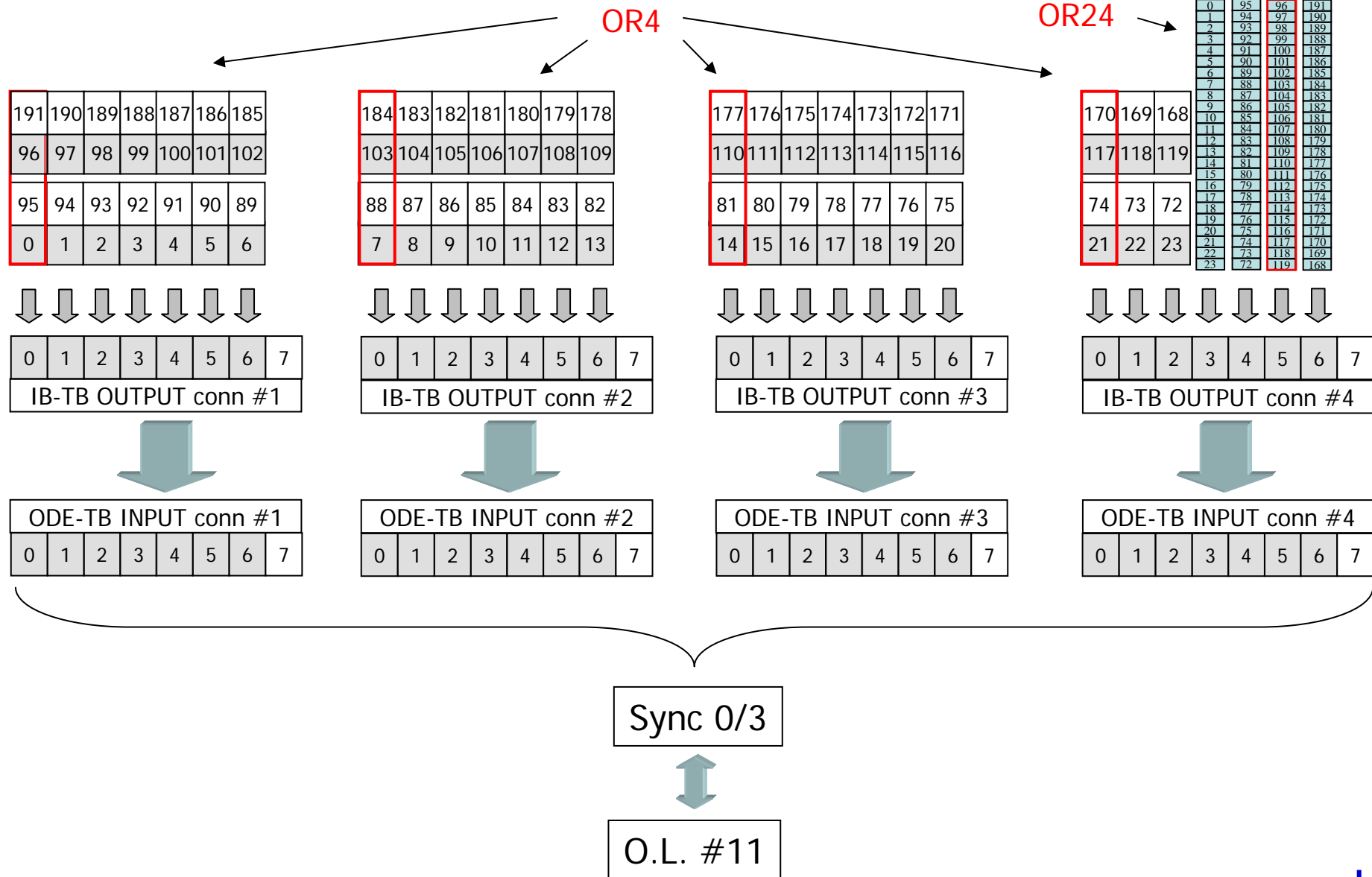


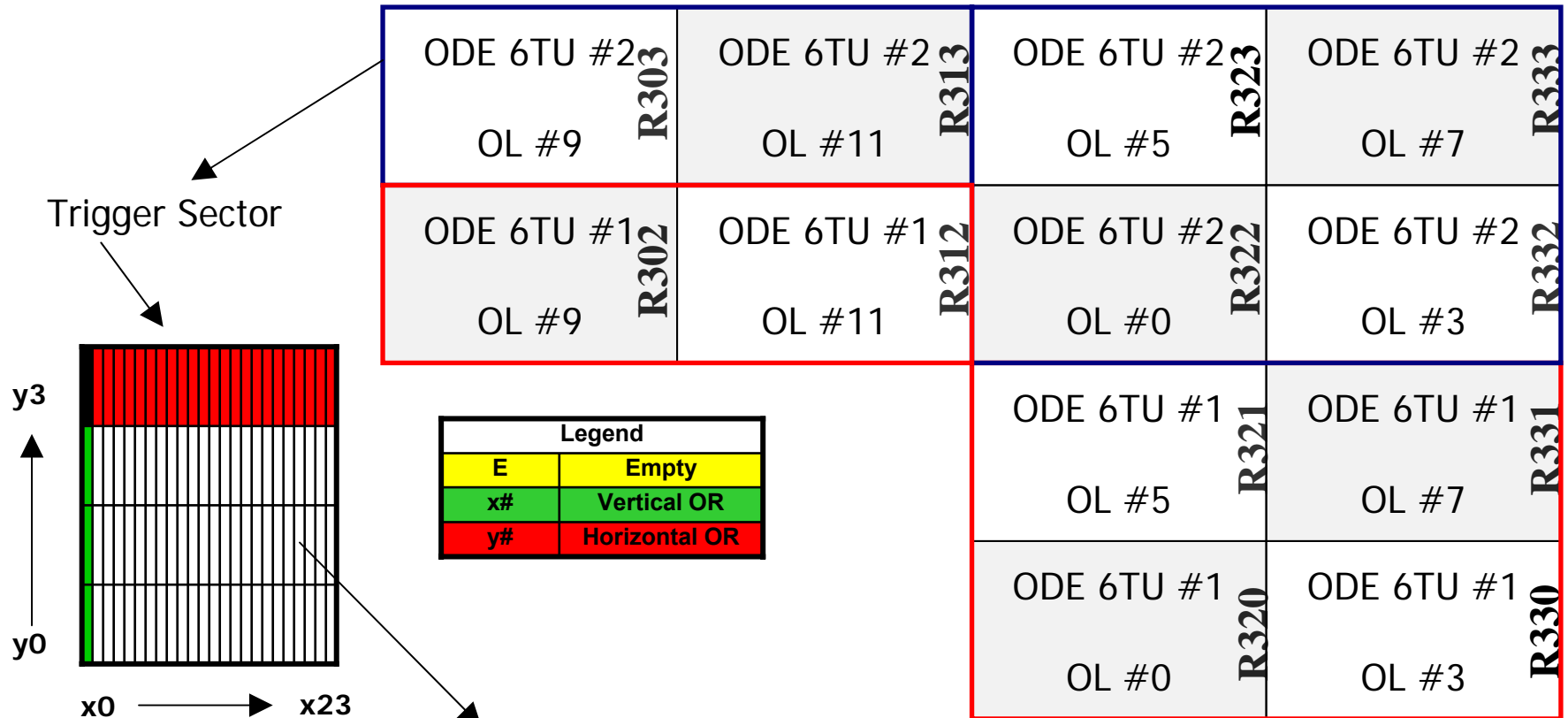












ODE-Optical Link Output Trigger Data Word

