Carioca design review report

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http://agenda.cern.ch/age?a03311

The reviewers would like to congratulate the Carioca design team for having prepared a well organized set of presentations for the review. The requirements to the Carioca front-end chip are especially demanding because of the large capacitance of the detectors and the large capacitance spread between different detector configurations. Because of the large detector capacitance the preamplifier is sensitive to noise sources in the microvolt range !. The demanding requirements to minimal dead time at high rates (up to 1MHz) from a wire signal with a long ion tail, and the fact that the chip must also handle positive and negative signals, are additional complications for the design. The current design seems to comply with most requirements with some characteristics that must be improved in the final version. The Carioca design has profited in many aspects from previously successful front-end chips for wire chambers (ASD for ATLAS MDT and ASDBLR for ATLAS TRT). The design of such a demanding analog front-end chip has been made additionally difficult by the fact that it has been designed by changing young designers (but highly motivated) with only limited support from experienced analog IC designers. The design team has in spite of these difficulties managed to design a chip that in the final version seems to be capable of coping with the very difficult requirements.

General comments to the chosen architecture

The traditional design approach to fulfill the requirements is a very linear preamplifier, a signal tail cancellation circuit which transforms the signal into a narrow unipolar pulse by means of a series of poles and zeros, which also cancels the return to zero of the preamplifier, and then a fast discriminator. The preamplifier needs to be quite linear over the signal range so that it does not introduce signal distortions, which would otherwise cause a mismatch between signal and tail cancellation circuit.

The preamplifier architecture chosen for the Carioca can be designed to return to zero quickly and to be quite robust. It is Though prone to non-linear behavior to a much larger degree than more traditional preamplifiers: two important sources of non-linearity exist in the feedback: the transistor n3 in the schematic governs the feedback and it sees a very large signal resulting in a time variation of its gm, and also the current mirror will, due to its limited output impedance, only mirror the current in an approximative, non-linear way. Due to this the return to zero of the preamp is non-linear, governed by transistor characteristics, and in addition also detector capacitance dependent. The cancellation of the tail of the preamp in the signal response by linear resistive and capacitive elements will therefore be approximative at best. Specifically it would be good to take another look at the Carioca preamp to reduce its non-linearity (gate signal of n3 and current mirror)

The topology of the Carioca preamplifier was originally proposed as a low noise technique to eliminate the feedback resistor in a usual transimpedance amplifier topology. By doing so, a lower noise can be achieved in cases where the feedback resistor is a dominant noise source as would be the case in low detector capacitance applications. The LHCb muon detector, however, does not fit into this category so the advantages of this topology are not clear. A feature of this topology is an input impedance which is not constant over frequency, and this results in variations of pulse shape with detector capacitance. For small detector capacitance, the pulse has a nice unipolar shape, while for large capacitance there is undershoot followed by low level ringing. The design team is aware of this effect, and while they find it annoying, it does not seem to prevent the design to obtain its required performance. Given the short schedule of the project, it does not make sense to attempt any major design changes in the preamp topology at this point.

Specific points

A gain difference from simulations of up to 50% for negative signals has been found while for positive signals a good match (18 %) to simulations has been obtained. Such a large discrepancy between simulations and prototypes must be understood as it may be the sign of an over sensitive design (to biasing conditions or alike). The problems seen (factor 10 gain decrease) in simulations of the circuit at increased temperature (100 deg.cent) must be understood as this could also be caused by marginal biasing conditions. The fact that such problems with simulations have been discovered so late in the design process gives some doubts if proper worst case simulations have been made systematically throughout the design process. Clear definitions of worst case corners must be made and the whole signal chain must be verified with these.

The internal signals related to the threshold levels and biasing could potentially benefit from some local decoupling, as these signals are intentional DC levels.

The main difficulty with the Carioca8 seems to be the coupling of noise from the digital sections (discriminator and LVDS cell) back into the input signal and the sensitive preamplifiers. When attached to a chamber, this results in sustained oscillations. The design team has found a way to solve this problem by loading the dummy preamp with a capacitance approximately equal to the detector capacitance as this ensures equal coupling into the two differential inputs. While this solution might solve the instability, it is not a very satisfying one. The effect seems to be caused by on-chip substrate ground bounce. Ground bounce during discriminator switching is coupled directly to the low resistivity substrate via a direct connection between digital ground and the substrate contacts of the digital cells. It is strongly recommended that this problem is addressed directly by isolating all substrate contacts in the discriminator and LVDS sections from the local “digital” ground bus and by providing a separate digital ground pad which does not connect to any substrate contacts. The designers are already planning additional on-chip power supply filtering which should also help. Its likely that with these changes, the system will be much more stable and robust, and the dummy capacitive loads may not be required. The production of front-end boards and their handling will be significantly easier if only one type of board will be needed. The planned exchange of the Standard-cell LVDS drivers (with some internal single ended signals) to a fully differential circuit may also bring improvements.

For very large detector capacitances >150 pF a common mode oscillation of the preamps can occur. It is a common mode oscillation not seen by the discriminator, but rendering the preamp unusable. A preliminary analysis made by the design team has revealed an issue with the voltage drop in the ground line of the preamp due to series resistance and inductance of the bonding wire when one of the 16 inputs receives a signal. This will be improved by increasing the widths of the corresponding line and have multiple bond pads and wires. Taking into account the capacitance value at which the oscillation currently starts and the need for some safety margin, an improvement in the preamp ground line of about a factor of 5 is envisaged.

The Carioca has not yet been tested in a package. All tests have been performed on directly bonded chips. The packaging of such a sensitive analog circuit could be critical and chips must have been tested in final packages before the design can be considered ready for a production. Testing of packaged chips should be started as early as possible

The chip will in the future support both common or individual thresholds but a quick decision must be taken for the Dialog chip supplying the thresholds. Using individual thresholds seems to be the safest approach, as it has not been demonstrated that the offsets can be sufficiently reduced.

One of the critical design parameters of the Carioca is the dead time from real and background hits. This is a critical parameter because of the chosen trigger scheme with a 5 out of 5 coincidence. An improved (faster) baseline restorer was included in the previous Carioca submission and was found to work satisfactory. It would be useful to get a good estimate of the effects on trigger efficiency if the effective dead time is increased to ~100ns instead of the initial design goal of 50ns.

The current time schedule with a final engineering run together with the Dialog and the Sync ASICs in the end of this year seems rather ambitious.